Chapter 4

SYSTEM MODULE

Original 07/97

CHAPTER 4 – SYSTEM MODULE

Contents

Introduction . . . . . Page 4–5
Technical Section . . . . . Page 4–5
External and Internal Connections . . . . . Page 4–5
External Connections . . . . . Page 4–5
System Connector X100 . . . . . Page 4–6
UI Connector X101 . . . . . Page 4–7
Flash Connector X103 . . . . . Page 4–8
SIM Connector X102 . . . . . Page 4–9
Baseband Block . . . . . Page 4–10
Introduction . . . . . Page 4–10
Modes of Operation . . . . . Page 4–11
Circuit Description . . . . . Page 4–11
Power Supply . . . . . Page 4–11
Charging Control Switch Functional Description . . . . . Page 4–12
Power Supply Regulator PSCLD, N301 . . . . . Page 4–14
PSCLD, N300 External Components . . . . . Page 4–14
PSCLD, N300 Control Bus . . . . . Page 4–15
Charger Detection . . . . . Page 4–16
SIM Interface and Regulator in N300 . . . . . Page 4–16
Power Up Sequence . . . . . Page 4–17
MCU . . . . . Page 4–19
MCU Access and Wait State Generation . . . . . Page 4–19
MCU Flash Loading . . . . . Page 4–20
Flash Prommer Connection Using Dummy Battery . . . . . Page 4–22
Flash, D400 . . . . . Page 4–22
SRAM D402, D403 . . . . . Page 4–22
EEPROM D401 . . . . . Page 4–22
MCU and Peripherals . . . . . Page 4–23
Baseband A/D Converter Channels usage in N450 and D150 Page 4–23
Battery Voltage Measurement . . . . . Page 4–24
Charger Voltage Measurement . . . . . Page 4–25
Battery Size Resistor Measurement . . . . . Page 4–25
Battery Temperature Measurement . . . . . Page 4–26
External Accessory Detection via XMIC/ID –line . . . . . Page 4–26
Keyboard Interface . . . . . Page 4–27
Keyboard and Display Light . . . . . Page 4–28
Audio Control . . . . . Page 4–28
Internal Audio . . . . . Page 4–29
External Audio . . . . . Page 4–30

DSP . . . . . Page 4–31
DSP Interrupts . . . . . Page 4–31
DSP Serial Communications Interface . . . . . Page 4–32
RFI2, N450 Operation . . . . . Page 4–32
SIM Interface . . . . . Page 4–33
Display Driver Interface . . . . . Page 4–35
RF Block . . . . . Page 4–37
Introduction . . . . . Page 4–37
Receiver . . . . . Page 4–37
Duplex Filter . . . . . Page 4–37
Pre–Amplifier . . . . . Page 4–38
RF Interstage Filter . . . . . Page 4–38
Diode Mixer . . . . . Page 4–38
IF Amplifier . . . . . Page 4–39
First IF Filter . . . . . Page 4–39
Receiver IF Circuit, RX part of CRFRT . . . . . Page 4–40
Second IF Filter . . . . . Page 4–40
Transmitter . . . . . Page 4–41
Modulator Circuit, TX part of CRFRT . . . . . Page 4–41
Upconversion Mixer . . . . . Page 4–42
TX amplifier . . . . . Page 4–43
TX Interstage Filters . . . . . Page 4–43
Power Amplifier . . . . . Page 4–44
Power control circuit . . . . . Page 4–44
Frequency Synthesizers . . . . . Page 4–45
VCTCXO . . . . . Page 4–45
VHF PLL . . . . . Page 4–46
VHF VCO + Buffer . . . . . Page 4–46
UHF PLL . . . . . Page 4–47
UHF VCO . . . . . Page 4–47
UHF VCO Buffer . . . . . Page 4–48
PLL Circuit . . . . . Page 4–48
Interconnection Diagram of Baseband . . . . . Page 4–49
Block Diagram of RF . . . . . Page 4–50
Power Distribution Diagram of RF . . . . . Page 4–51
GJ8: Block Diagram of Baseband . . . . . Page 4–52
GJ8: Circuit Diagram of Power Supply & Charging . . . . . Page 4–53
GJ8: Circuit Diagram of Central Processing Unit . . . . . Page 4–54
GJ8: Circuit Diagram of MCU Memory Block . . . . . Page 4–55
GJ8: Circuit Diagram of Keyboard & Display Interface . . . . . Page 4–56
GJ8: Circuit Diagram of Audio . . . . . Page 4–57

GJ8: Circuit Diagram of DSP Memory Block . . . . . Page 4–58
GJ8: Circuit Diagram of RFI . . . . . Page 4–59
GJ8: Circuit Diagram of Receiver . . . . . Page 4–60
GJ8: Circuit Diagram of Transceiver . . . . . Page 4–61
GJ8: Circuit Diagram of System Connector . . . . . Page 4–62
Layout Diagrams of GJ8 (Version: 15) . . . . . Page 4–63
GJ8A: Block Diagram of Baseband . . . . . Page 4–64
GJ8A: Circuit Diagram of Power Supply & Charging . . . . . Page 4–65
GJ8A: Circuit Diagram of Central Processing Unit . . . . . Page 4–66
GJ8A: Circuit Diagram of MCU Memory Block . . . . . Page 4–67
GJ8A: Circuit Diagram of Keyboard & Display Interface . . . . . Page 4–68
GJ8A: Circuit Diagram of Audio . . . . . Page 4–69
GJ8A: Circuit Diagram of DSP Memory Block . . . . . Page 4–70
GJ8A: Circuit Diagram of RFI . . . . . Page 4–71
GJ8A: Circuit Diagram of Receiver . . . . . Page 4–72
GJ8A: Circuit Diagram of Transceiver . . . . . Page 4–73
GJ8A: Circuit Diagram of System Connector . . . . . Page 4–74
Layout Diagrams of GJ8A (Version: 02) . . . . . Page 4–75
Parts list of GJ8 (EDMS Issue 8.8 Code: 0200591 for layout 15) Page 4–76
Parts list of GJ8A (EDMS Issue 4.1 Code: 0201017 for layout 02) Page 4–89

Introduction

The GJ8A is the RF module of the NHE–6 cellular transceiver. The GJ8A module carries out all the RF and system functions of the transceiver. This module works in the GSM system.

Technical Section

The GJ8A module is constructed on a 1.0 mm thick FR4 eight–layer printed wiring board. The dimensions of the PWB are 126 mm x 43 mm.

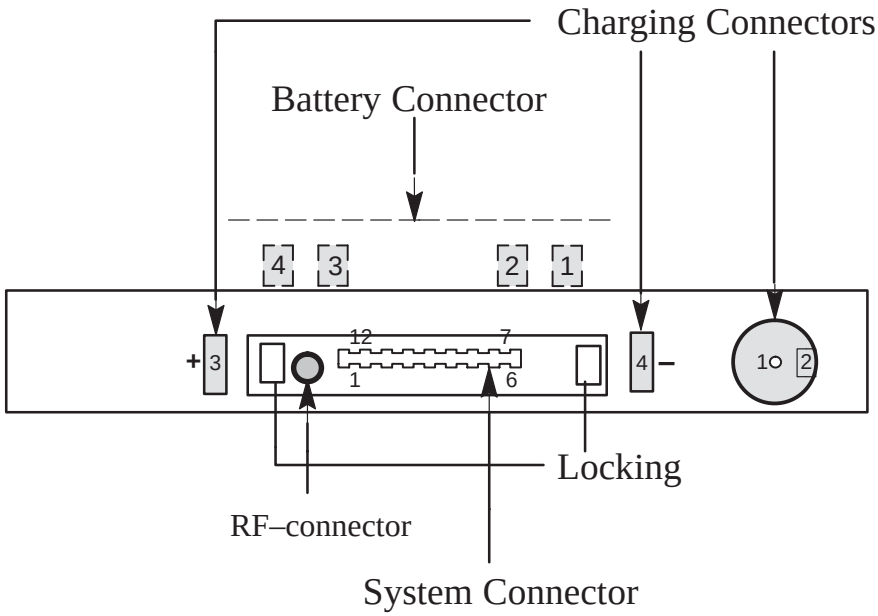
Components are located on both sides of the PWB. The RF components are located on the top end of the PWB. The both sides of the board includes high and low components. The maximum usable height is 5 mm.

EMI leakage is prevented by a metallized plastic (or magnesium) shield A on side 1/8 and a meatallized plastic cover B on side 8/8. The shield A also conducts the heat out of the inner parts of the phone, thus preventing excessive temperature rise.

External and Internal Connections

The system module has two connector, external bottom connector and internal display module connector.

External Connections



System Connector X100

Accessory Connector

Pin:	Name:	Description:
1	GND	Charger/system ground
2	V_OUT	Accessory output supply • min/typ/max: 3.40...10 V (output current 50 mA)
3	XMIC ID	External microphone input and accessory identification • typ/max: 8...50 mV (the maximum value corresponds to 0 dBm network level with input amplifier gain set to 20 dB, typical value is maximum value –16 dB) Accessory identification • 1.7...2.05 V headset adapter connected • 1.15...1.4 V compact handsfree unit connected • 2.22... 2.56 V Infra Red Link connected
4	EXT_RF	External RF control input • min/max: 0...0.5 V External RF in use • min/max: 2.4...3.2 V Internal antenna in use
5	TX	FBUS transmit
6	MBUS	Serial control bus • logic low level: 0...0.5 V • logic high level: 2.4...3.2 V
7	BENA	No connection
8	SGND	Signal ground
9	XEAR	External speaker and mute control • min/nom/max: 0...32...500 mV (typical level corresponds to –16 dBm0 network level with volume control in nominal position 8 dB below maximum. Maximum 0 dBm0 max. volume codec gain –6 dB) • mute on (HF speaker mute): 0...0.5 V d.c. • mute off (HF speaker active): 1.0...1.7 V d.c.
10	HOOK	Hook signal • hook off (handset in use) : 0...0.5 V • hook on, (handset not in use): 2.4...3.2 V
11	RX	FBUS receive • accessory FBUS receive signal,
12	V_IN	Charging supply voltage

Battery Connector

Pin:	Name:	Description:
13	BGND	Battery ground
14	BSI	Battery size indicator (used also for SIM card detection)
15	BTEMP	Battery temperature (used also for vibration alert)
16	VB	Battery voltage • min/typ/max: 5.3...6...10.26 V

Charging connectors

Pin:	Name:	Description:
12,17,19	V_IN	Charging voltage input • ACH–6 min/nom/max: 9.8...10.3...10.8 V • ACH–8 min/nom/max: 12...14...16 V
18, 20	GND	Charger/system ground

UI Connector X101

Pin:	Name:	Description:
1	MICP	Microphone • min/typ/max: 0...2...12.5 mV Connected to Audio Codec Microphone input. The maximum value corresponds to 1 kHz, o dBmO network level input amplifier gain set to 32 dB. Typical value is maximum value –16 dB.
2	MICN	Microphone • min/max: 0...12.5 mV Connected to Audio Codec and over resistor to AGND
3	GND	Ground
4	VL	Display supply • min/max: 3.0...3.2 mV
5	SYSRESETX	Reset, Level sensitive
6	GND	Ground
7	KEYLIGHT	Keyboard Light

Pin:	Name:	Description:
8	LCDLIGHT	Display light
9	BUZZER	PWM signal Buzzer control
10	GND	Ground
11	SLIDEON	Slide indication
12	GENSCLK	Serial clock
13	GENSD	Serial data
14	LCDENX	LCD enable
15	VB	Battery supply
16	XPWRON	Power ON/OFF
17	EARN	Earphone • min/typ/max: 0...14...220 mV. Connected to Audio Codec Inverted Output. Typical level corresponds to –16 dBmO network level with volume control giving nominal RLR (=+2 dB) 8 dB below max. Max level is 0 dBmO with max volume (codec gain –11 dB).
18	EARP	Earphone (see above)
19	CALL_LED	Call indication led
20–25	ROW(0–5)	
26–29	COL(0–4)	
30	GND	Ground

Flash Connector X103

Pin:	Name:	Description:
1	VPP	Flash programming voltage • min/typ/max: 11.4...12...12.6 V (values when VPP active), test point J310
2	FRX	Flash data receive, test point J311
3	FTX	Flash acknowledge transmit, test point J312
4	FCLK	Flash serial clock, test point J313
5	WDDIS	Watchdog disable, signal pulled down to disable watchdog, test point J314
6	GND	Digital ground, test point J315

SIM Connector X102

Pin:	Name:	Description:
1	GND	Ground for SIM
2	VSIM	SIM voltage supply • min/typ/max: 4.8...4.9...5.0 V
3	SDATA	Serial data for SIM
4	SRES	Reset for SIM
5	CLK	Clock for SIM data (clock frequency minimum 1 MHz if clock stopping not allowed)

Baseband Block

Introduction

The GJ8A module is used in GSM products. The baseband is implemented using DCT2 core technology. The baseband is built around one DSP, System ASIC and the MCU. The DSP performs all speech and GSM related signal processing tasks. The baseband power supply is 3V except for the A/D and D/A converters that are the interface to the RF section. The A/D converters used for battery and accessory detection are integrated into the same device as the signal processing converters.

The audio codec is a separate device which is connected to both the DSP and the MCU. The audio codec support the internal and external microphone/earpiece functions. External audio is connected in a dual ended fashion to improve audio quality together with accessories.

The baseband implementation support a 32.768 kHz sleep clock function for power saving. The 32.768 kHz clock is used for timing purposes during inactive periods between paging blocks. This arrangement allows the reference clock, derived from RF to be switched off.

The baseband clock reference is derived from the RF section and the reference frequency is 13 MHz. A low level clipped sinusoidal wave form is fed to the ASIC which acts as the clock distribution circuit. The DSP is running at 39 MHz using an internal PLL. The clock frequency supplied to the DSP is 13 MHz. The MCU bus frequency is the same as the input frequency. The system ASIC provides both 13 MHz and 6.5 MHz as alternative frequencies. The MCU clock frequency is programmable by the MCU. The NHE–6 baseband uses 13 MHz as the MCU operating frequency. The RF A/D, D/A converters are operated using the 13 MHz clock supplied from the system ASIC

The power supply and charging section supplies Lithium type of battery technology. The battery charging unit is designed to accept constant current type of chargers, that are approved by NMP.

The power supply IC contains three different regulators. The output voltage from each regulator is 3.15V nominal. One of the regulator uses an external transistor as the boost transistor.

Modes of Operation

The baseband operates in the following Modes

– Active, as during a call or when baseband circuitry is operating

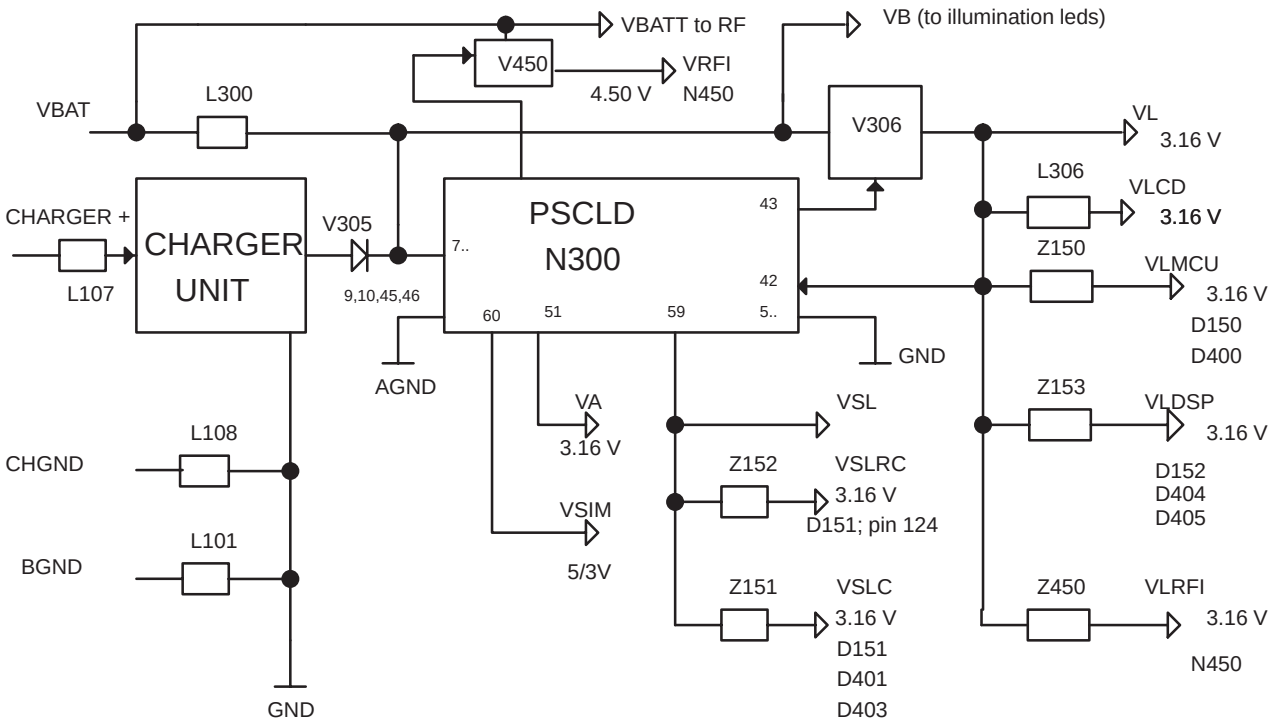
– Sleep, in this mode the clock to the baseband is stopped and timing is kept by the 32.768 kHz oscillator. All Baseband circuits are powered

– Acting dead, in this mode the battery is charged, but only necessary functions for charging are running

– Power off, in this mode all baseband circuits are powered off. The regulator IC N300 is powered

Circuit Description

Power Supply



The power supply for the baseband is the main battery. The main battery consists of 2 LI–ION cells. A charger input is used to charge the battery. Two different chargers can be used for charging the battery. A switch mode type fast charger that can deliver 780 mA and a standard charger that can deliver 265 mA. Both chargers are of constant current type.

The baseband has one power supply circuit, N300 delivering power to the different parts in the baseband. There are two logic power supply and one analog power supply. The analog power supply VA is used for analog circuits such as

audio codec, N200 and microphone bias circuitry. Due to the current consumption and the baseband architecture the digital supply is divided into two parts.

Both digital power supply rails from the N300, PSCLD are used to distribute the power dissipation inside N300, PSCLD. The main logic power supply VL has an external power transistor, V306 to handle the power dissipation that will occur when the battery is fully charged or during charging.

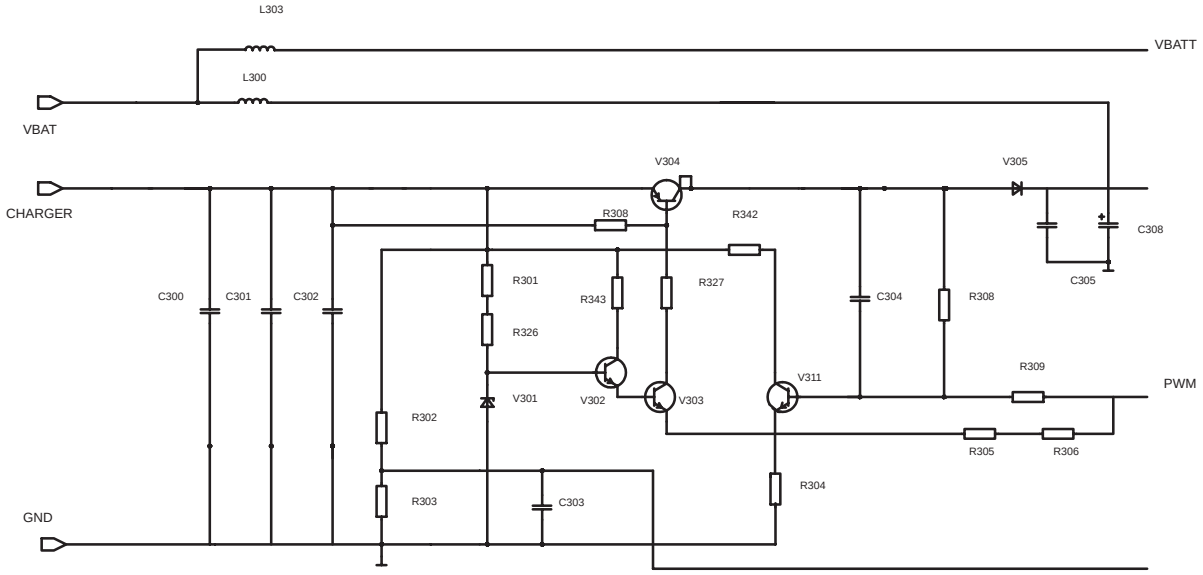
D151, ASIC and the MCU SRAM, D403 are connected to the same logic supply voltage. All other digital circuits are connected to the main digital supply. The analog voltage supply is connected to the audio codec.

Charging Control Switch Functional Description

The charging switch transistor V304 controls the charging current from the charger input to the battery. During charging the transistor is forced in saturation and the voltage drop over the transistor is 0.2–0.4V depending upon the current delivered by the charger. Transistor V304 is controlled by the PWM output from N300, pin 34 via resistors R309, R308 and transistor V311. The output from N300 is of open drain type. When transistor V304 is conducting the output from N300 pin is low. In this case resistors R305 and R306 are connected in parallel with R304. This arrangement increases the base current thru V304 to put it into saturation.

Transistors V304, V302, V303 and V311 forms a simple voltage regulator circuitry. The reference voltage for this circuitry is taken from zener diode V301. The feedback for the regulator is taken from the collector of V304. When the PWM output from N300 is active, low, the feedback voltage is determined by resistors R308 and R309. This arrangement makes the charger control switch circuitry to act as a programmable voltage regulator with two output voltages depending upon the state of the PWM output from N300. When the PWM is inactive, in high impedance the feedback voltage is almost the same as on the collector of V304. Due to the connection the voltage on V303 and V311 emitters are the same. The influence of the current thru R305 and R306 can be neglected in this case.

The charging switch circuit diagram is shown in following figure. The figure is for reference only.



This feedback means that the system regulates the output voltage from V304 in such a way that the base of V303 and V311 are at the same voltage. The voltage on V302 is determined by the V301 zener voltage. The darlington connection of V303 and V302 service two purposes ; 1 the load on the voltage reference V301 is decreased, 2 the output voltage on V304 is decreased by the VBE voltage on V302 which is a wanted feature. The voltage reduction allows a relative temperature stable zener diode to be used and the output voltage from V304 is at a suitable level when the PWM output from N300 is not active.

The circuitry is self starting which means that an empty battery is initially charged by the regulator circuitry around the charging switch transistor. The battery is charged to a voltage of maximum 4.8V. This charging switch circuitry allows for both NiCd, NiMH and Lithium type of batteries to be used.

When the PWM output from N300 is active the feedback voltage is changed due to the presence of R308 and R309. When the PWM is active the charging switch regulator voltage is set to 10.5V maximum. This means that even if the voltage on the charger input exceeds 11.5V the battery voltage will not exceed 10.5 V. This protects N300 from over voltage even if the battery was to be detached while charging.

The RC network C304, R308 and R309 also acts as a delay circuitry when switching from one output voltage to an other. This happens when the PWM output from N300 is pulsing. The reason for the delay is to reduce the surge current that will occur when V304 is put into conducting state. Before V304 is put in conducting state there is a significant voltage drop over V304. The energy is stored in capacitors in the charger and these capacitors must first be drained in order to put the charger in constant current mode. This is done by discharging the capacitors into the battery. The delay caused by C304 will reduce the surge current thru V304 to an acceptable value.

R301 and R326 are used to regulate the zener current. During charging with empty battery the zener voltage might drop due to low zener current but this is no problem since the regulator is operating in constant current mode while

charging. The zener voltage is more important when the charger voltage is high or in case that the PWM output from N300 is inactive. In this case the charger idle voltage is present at the charger supply pins.

R300 and R327 together with V304 forms a constant current source. The surge current limitation behavior is frequency dependent since L107 is an inductor. The purpose of these circuits is to reduce the surge current through V304 when it is put in conducting state. Due to the low resistance value required in L107 this arrangement is not very effective and the RC network R308, R309 and C304 contributes more to the surge current reduction.

V305 is a schottky diode that prevents the battery voltage from reverse bias V304 when the charger is not connected. The leakage current for V305 is increasing with increasing temperature and the leakage current is passed to ground via R308, V311 and R304. This arrangement prevents V304 from being reversed biased as the leakage current increases at high temperatures.

Components L107, C300, C301, C302 and L108 forms a filter for EMC attenuation. The circuitry reduces the conductive EMC part from entering the charger cable causing an increase in emission as the cable will act as an antenna.

V100 is a 18V transient suppressor. V100 protects the charger input and in particular V304 for over voltage. The cut off voltage is 18V with a maximum surge voltage up to 25V. V100 also protects the input for wrong polarity since the transient suppressor is bipolar.

Power Supply Regulator PSCLD, N301

The power supply regulators are integrated into the same circuit N300. The power supply IC contains three different regulators. The main digital power supply regulator is implemented using an external power transistor V306. The other two regulators are completely integrated into N300.

PSCLD, N300 External Components

N300 performs the required power on timing. The PSCLD, N300 internal power on and reset timing is defined by the external capacitor C330. This capacitor determines the internal reset delay, which is applied when the PSCLD, N300 is initially powered by applying the battery. The baseband power on delay is determined by C311. With a value of 10 nF the power on delay after a power on request has been active is in the range of 50–150 ms. C310 determines the PSCLD, N300 internal oscillator frequency and the minimum power off time when power is switched off.

The sleep control signal from the ASIC, D151 is connected via PSCLD, N300. During normal operation the baseband sleep function is controlled by the ASIC, D151 but since the ASIC is not power up during the startup phase the sleep signal is controlled by PSCLD, N300 as long as the PURX signal is active. This arrangement ensures that the 13 MHz clock provided from RF to the ASIC, D151 is started and stable before the PURX signal is released and the base-

band exits reset. When PURX is inactive, high, sleep control signal is controlled by the ASIC D151.

To improve the performance of the analog voltage regulator VA an external capacitor C329 has been added to improve the PSRR.

N300 requires capacitors on the input power supply as well as on the output from each regulator to keep each regulator stable during different load and temperature conditions. C305 and C308 are the input filtering capacitors. Due to EMC precautions a filter using C305, L300 and C308 has been inserted into the supply rail. This filter reduces the high frequency components present at the battery supply from exiting the baseband into the battery pack. The regulator outputs also have filter capacitors for power supply filtering and regulator stability. A set of different capacitors are used to achieve a high bandwidth in the suppression filter.

PSCLD, N300 Control Bus

The PSCLD, N300 is connected to the baseband common serial control bus, SCONB(5:0). This bus is a serial control bus from the ASIC, D151 to several devices on the baseband. This bus is used by the MCU to control the operation of N300 and other devices connected to the bus. N300 has two internal 8 bit registers and the PWM register used for charging control. The registers contains information for controlling reset levels, charging HW limits, watchdog timer length and watchdog acknowledge.

The control bus is a three wire bus with chip select for each device on the bus and serial clock and data. From PSCLD, N300 point of view the bus is used as write only to PSCLD. It is not possible to read data from PSCLD, N300 by using this bus.

The MCU can program the HW reset levels when the baseband exits/enters reset. The programmed values remains until PSCLD is powered off, the battery is removed. At initial PSCLD, N300 power on the default reset level is used. The default value is 5.1 V with the default hysteresis of 400 mV. This means that reset is exit at 5.5 V when the PSCLD, N300 is powered for the first time.

The watchdog timer length can be programmed by the MCU using the serial control bus. The default watchdog time is 32 s with a 50 % tolerance. The complete baseband is powered off if the watchdog is not acknowledged within the specified time. The watchdog is running while PSCLD, N300 is powering up the system but PURX is active. This arrangement ensures that if for any reason the battery voltage doesn’t increase above the reset level within the watchdog time the system is powered off by the watchdog. This prevents a faulty battery from being charged continuously even if the voltage never exceeds the reset limit. As the time PURX is active is not exactly known, depends upon startup condition, the watchdog is internally acknowledged in PSCLD when PURX is released. This gives the MCU always the same time to respond to the first watchdog acknowledge.

Baseband power off is initiated by the MCU and power off is performed by writing the smallest value to the watchdog timer register. This will power off the baseband within 0.5 ms after the watchdog write operation.

The control bus can also be used to setup the behavior of the N300 regulators during sleep mode, when sleep signal is active low. In order to reduce power during sleep mode two of the three regulators can be switched off. The third regulator, VSL which is kept active then supplies the output of the other regulators. All regulator outputs from PSCLD, N300 are supplied but the current consumption is restricted. It is also possible to keep the VL regulator active during sleep mode in case the power consumption is in excess of what the VSL regulator can deliver in sleep mode to the VL output.

The PSCLD, N300 also contains switches for connecting the charger voltage and the battery voltage to the base band A/D converters. Since the battery voltage is present and the charger voltage might be present in power off the A/D converter signals must be connected using switches. The switch state can be changed by the MCU via the serial control bus. When PURX is active both switches are open to prevent battery/charger voltage from being applied to the baseband measurement circuitry which is powered off. Before any measurement can be performed both switches must be set in not closed mode by MCU.

Charger Detection

A charger is detected if the voltage on N300 pin 41 is higher than 0.5V. The charger voltage is scaled externally to PSCLD, N300 using resistors R302 and R303. With the implemented resistor values the corresponding voltage at the charger input is 2.8V. Due to the multi–function of the charger detection signal from PSCLD, N300 to ASIC, D151 the charger detection line is not forced, active high until PURX is inactive. In case PURX is inactive the charger detection signal is directly passed to D151. The active high on pin 21 generates and interrupt to MCU which then starts the charger detection task in SW.

The reason for not passing the charger detection signal to the ASIC, D151 when PURX is active is the RTC implementation in ASIC, D151. This same signal is used to power up the system if the RTC alarm is activated and the system is power up. Due to this the PSCLD, N300 pin 21 is in input mode as long as PURX is active. Correspondingly at the ASIC end this pin is an output as long as PURX is active. The RTC function needs SW support and is not implemented in NHE–6. The baseband architecture provides for the functionality required.

SIM Interface and Regulator in N300

The SIM card regulator and interface circuitry is integrated into PSCLD, N300. The benefit from this is that the interface circuits are operating from the same supply voltage as the card, avoiding the voltage drop caused by the external switch used in previous designs. The PSCLD, N300 SIM interface also acts as voltage level shifting between the SIM interface in the ASIC, D151 operating at 3V and the card operating at 5V. Interface control in PSCLD is direct from

ASIC, D151 SIM interface using SIM(5:0) bus. The MCU can select the power supply voltage for the SIM using the serial control bus. The default value is 3V which can be changed to 5V by the SIM interface in ASIC, D151. Regulator enable and disable is controlled by the ASIC via SIM(2).

Power Up Sequence

The baseband can be powered up in three different ways.

– When the power switch is pressed input pin 37 to PSCLD, N300 is connected to ground and this switches on the regulators inside PSCLD.

– An other way to power up is to connect the charger. Connecting the charger causes the baseband to power up and start charging the battery.

– The third way to power the system up is to attach the battery.

Power up using Power on Button

This is the most common way to power the system up. This power up is successful if the battery voltage is higher than power on reset level set by the MCU, default value 5.4 V DC in PSCLD, N300. The power up sequence is started when the power on input pin 37 at PSCLD is activated, low. The PSCLD then internally enters the reset state where the regulators are switched on. At this state the PWM output (pin 34) from PSCLD is forced active to support additional power from any charger connected. The sleep control output signal is forced high enabling the regulator to supply the VCO and startup the clock. After the power on reset delay of 50–150 ms PURX is released and the system exits reset. The PWM output is still active until the MCU writes the first value to the PWM register. The watchdog has to be acknowledged within 16 s after that PURX has changed to inactive state

Power Up with Empty Battery using Charger

When the charger is inserted into the DC jack or charger voltage is supplied at the system connector contacts/pins, PSCLD (N300) powers up the baseband. The charging control switch is operating as a linear regulator, the output voltage is 4.5V–5V. This allows the battery to be charged immediately when the charger is connected. This way of operation guarantees successful power up procedure with empty battery. In case of empty battery the only power source is the charger. When the battery has been initially charged and the voltage is higher than the PSCLD, N300 switch on voltage the sleep control signal which is connected to the PSCLD for power saving function sleep mode, enters inactive state, high, to enable the regulator that controls the power supply to the VCO to be started. The ASIC, D151 which normally controls the sleep control line has the sleep output inactive, low as long as the system reset, PURX is active, low, from PSCLD. After a delay of about 5–10 ms the system reset output PURX from PSCLD enters high state. This delay is to ensure that the clock is stable when the ASIC exits reset. The sleep control output from the PSCLD that has been driving an output until now, returns the control to the sleep signal from the ASIC as the PURX signal goes inactive. When the PURX signal goes inactive, high, the charge detection output at PSCLD, that is in input mode when

PURX is active, switches to output and goes high indicating that a charger is present. When the system reset, PURX, goes high the sleep control line is forced inactive, high, by the ASIC, D151 via PSCLD, N300.

Once the system has exited reset the battery is initially charged until the MCU writes a new value to the PWM in PSCLD. If the watchdog is not acknowledged the battery charging is switched off when the PSCLD shuts off the power to the baseband. The PSCLD will not enter the power on mode again until the charger has been extracted and inserted again or the power switch has been pressed. The battery is charged as long as the power on line, PWRONX is active low. This is done to allow the phone to be started manually from the power button when the charger is connected and there is no need to disconnect the charger to get a power up if the battery is empty.

Power On Reset Operation

The system power up reset is generated by the regulator IC, N300. The reset is connected to the ASIC, D151 that is put into reset whenever the reset signal, PURX is low. The ASIC (D151) then resets the DSP (D152) the MCU (D150) and the digital parts in RFI2 (N450). When reset is removed the clock supplied to the ASIC, D151 is enabled inside the ASIC. At this point the 32.768 kHz oscillator signal is not enabled inside the ASIC, since the oscillator is still in the startup phase. To start up the block requiring 32.768 kHz clock the MCU must enable the 32.768 kHz clock. The MCU reset counter is now started and the MCU reset is still kept active, low. 6.5 MHz clock is started to MCU in order to put the MCU(D150) into reset, MCU is a synchronous reset device and needs clock to reset. The reset to MCU is put inactive after 128 MCU clock cycles and MCU is started.

DSP (D152) and RFI2 (N450) reset is kept is kept active when the clock inside the ASIC, D151 is started. 13 MHz clock is started to DSP (D152) and puts it into reset. D152 is a synchronous reset device and requires clock to enter reset. N450 digital parts are reset asynchronously and do not need clock to be supported to enter reset.

As both the MCU, D151 and DSP, D152 are synchronous reset devices all interface signals connected between these devices and ASIC D151 which are used as I/O are set into input mode on the ASIC, D151 side during reset. This avoids bus conflicts to occur before the MCU, D150 and the DSP, D152 are actually reset.

The DSP (D152) and RFI2 (N450) reset signal remains active after that the MCU has exited reset. The MCU write to the ASIC register to disable the DSP reset. This arrangement allows the MCU to reset the DSP, D152 and RFI2, N450 when ever needed. The MCU can put DSP into reset by writing the reset active in the ASIC, D151 register.

MCU

The baseband used a Hitachi H3001 type of MCU. This is a 16–bit internal MCU with 8–bit external data bus. The MCU is capable of addressing up to 16 Mbyte of memory space linearly depending upon the mode of operation. The MCU has a non multiplexed address/data bus which means that memory access can be done using less clock cycles thus improving the performance but also tightening up memory access requirements. The MCU is used in mode 3 which means 8–bit external data bus and 16 Mbyte of address space. The MCU operating frequency is equal to the supplied clock frequency. The MCU has 512 bytes of internal SRAM. The MCU has one serial channel, USART that can operate in synchronous and asynchronous mode. The USART is used in the MBUS implementation. Clock required for the USART is generated by the internal baud rate generator. The MCU has 5 internal timers that can be used for timing generation. Timer TIOCA0 input pin 71 is used for generation of netfree signal from the MBUS receive signal which is connected to the MCU USART receiver input on pin 2.

The reason for generating the MBUS netfree using the counter is the fact that the 32.768 kHz clock that would have been used for this timing is a slow starting oscillator. This means that in production testing the MBUS can not be operated until the netfree counter is operational. As the netfree counter is implemented using the MCU internal counter the netfree counter is available immediately after reset. In the same way the MCU OS timer is operated from an internal timer in the early stage until the 32.768 kHz clock can be enabled and the OS timer provided in the ASIC can be used.

The MCU contains 4 10–bit A/D converters channels that are used for baseband monitoring.

The MCU, D150 has several programmable I/O ports which can be configured by SW. Port 4 which multiplexed with the LSB part of the data bus is used baseband control. In the mode the MCU is operating this port can be used as an I/O port and not as part of the data bus, D0–D7.

MCU Access and Wait State Generation

The MCU can access external devices in 2 state access or 3 state access. In two state access the MCU uses two clock cycles to access data from the external device. In 3 state access the MCU uses 3 clock cycles to access the external device or more if wait states are enabled. The wait state controller can operate in different modes. In this case the programmable wait mode is used. This means that the programmed amount of wait states in the wait control register is inserted when an access is performed to a device located in that area. The complete address space is divided into 8 areas each area covering 2 Mbyte of address space. The access type for each area can be set by bits in the access state control register. Further more the wait state function can be enabled separately for each area by the wait state controller enable register. This means that in 3 state access two types of access can be performed with a fixed setting:

– 3 state access without wait states
– 3 state access with the amount of wait states inserted determined by the wait control register

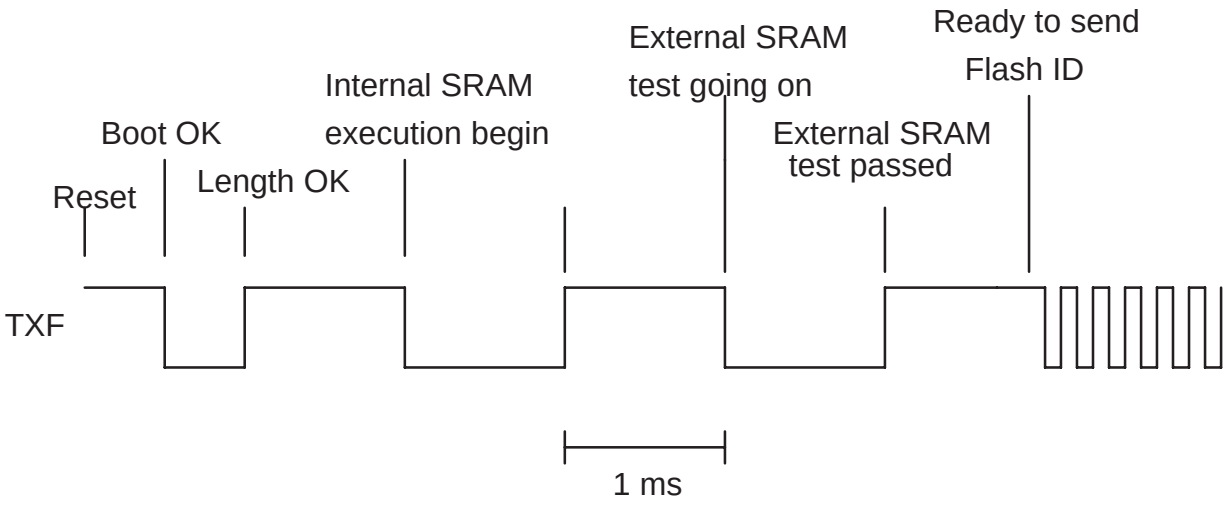
If the wait state controller is not enabled for a 3 state access area no waits states are inserted when accessing that area even if the wait control register contains a value that differs from 0 states.

MCU Flash Loading

MCU Boots from ASIC ROM. The flash loading equipment is connected to the baseband by means of the test connector before the module is cut out from the frame. Updating SW on a final product is done by removing the battery and connect a special battery that contains the necessary contacting elements. The contacts on the baseband board are test points that are accessible when the battery is detached. The power supply for the base band is supplied via the adapter and controlled by the flash programming equipment. The base band module is powered up when the power is connected to the battery contact pins.

The interface lines between the flash prommer and the baseband are in low state when power is not connected by the flash prommer. The data transfer between the flash programming equipment and the base band is synchronous and the clock is generated by the flash prommer. The same USART that is used for MBUS communication is used for the serial synchronous communication. The PSCLD watchdog is disabled when the flash loading battery pack and cable is connected.

After the flash battery pack adapter has been mounted or the test connector has been connected to the board the power to the base band module is connected by the flash prommer or the test equipment. All interface lines are kept low except for the data transmit from the baseband that is in reception mode on the flash prommer side, this signal is called TXF. The MCU boots from ASIC and investigates the status of the synchronous clock line. If the clock input line from the flash prommer is low or no valid SW is located in the flash MCU forces the initially high TXF line low acknowledging to the flash prommer that it is ready to accept data . The flash prommer sends data length, 2 bytes, on the RXF data line to the baseband. The MCU acknowledges the 2 data byte reception by pulling the TXF line high. The flash prommer now transmits the data on the RXF line to the MCU. The MCU loads the data into the internal SRAM. After having received the transferred data correctly MCU puts the TXF line low and jumps into internal SRAM and starts to execute the code. After a guard time of 1 ms the TXF line is put high by the MCU. After 1 ms the TXF is put low indicating that the external SRAM test is going on. After further 1 ms the TXF is put high indicating that external SRAM test has passed. The MCU performs the flash memory identification based upon the identifiers specified in the Flash Programming Specifications. In case of an empty device, identifier locations shows FFH, the flash device code is read and transmitted to the Flash Prommer. The TXF line functional timing is shown in the following diagram.



After that the device mounted on base band has been identified the Flash Prommer down loads the appropriate algorithm to the baseband. The programming algorithm is stored in the external SRAM on the baseband module and after having down loaded the algorithm and data transfer SW, MCU jumps to the external SRAM and starts to execute the code. The MCU now asks the prommer to connect the flash programming power supply. This SW loads the data to be programmed into the flash and implements the programming algorithm that has been down loaded.

Flash Prommer Connection Using Dummy Battery

For MCU SW updating in the field a special battery adapter can be used to connect to the test points which are accessible through SIM opening in the chassis, located behind the battery. Supply voltage must be connected to this dummy battery as well as the flash programming equipment

Flash, D400

A 8 MBit flash is used as the main program memory, D400 the device is 3 V read/program with external 12V VPP for programming. The device is sectored and contains 16 64 kByte blocks. The sector capability is not used in the HD843 application. The speed of the device is 180 ns. The MCU operating at 13 MHz will access the flash in 3 state access, requiring 190 ns access time from the memory.

The flash has a deep power down mode that can be used when the device is not active. There is a requirement for a longer access time if the device is accessed immediately after exiting power down. This requirement is met since the signal controlling the VCO power control is used for this purpose. The flash power down pin, pin 12 is connected to ASIC, D151 pin 130. The reason for connecting it to the ASIC and not direct to the VCO power control signal is that this pin on the ASIC is low as long as the ASIC is in reset. This signal also resets the flash memory as this pin also acts as a power up reset to the memory.

SRAM D402, D403

The baseband is designed to use SRAM size 128kx8. The required speed is 100 ns as the MCU will operate at 13 MHz and the SRAM will be accessed in 3 state access. The SRAM has no battery backup which means that the content is lost even during short power supply disconnections. As shown in the memory map the SRAM is not accessible after boot until the MCU has enabled the SRAM access by writing to the ASIC register.

EEPROM D401

The baseband is designed to use an 8kx8 parallel EEPROM.

The parallel device is connected to the MCU data and address bus. The ASIC generates chip select for the EEPROM. To avoid unwanted EEPROM access there is an EEPROM access bit in the ASIC MCU interface. This bit mus be set to allow for EEPROM access. This bit is cleared by default after reset. After each access this bit should be cleared to prevent unwanted EEPROM access. The parallel device used support page mode writing, 64 byte page. One page can be written by the MCU and after that the internal programming procedure is started. The page write operation is internally timed in the device and consecutive bytes must be written within 150 us. During this operation all interrupts must be disabled.

The device also supports SW protection to prevent accidental write operations to the device. The protection algorithm can be enabled and disabled by writing a predefined sequence to the device. Writing to the device while protected can be done by first writing the key sequence followed by the data.

MCU and Peripherals

MCU Port P4 Usage

MCU, D150 port 4 is used for baseband control.

Port Pin	MCU pin	Control Function	Remark
P40	5	Display driver reset	Active low
P41	6		
P42	7	Call Led Control	
P43	8	External RF Switch input	
P44	9		
P45	10		
P46	11		
P47	12	External accessory Supply voltage control	Active low

MCU Port PB Usage

MCU, D150 port B is used for baseband control.

Port Pin	MCU pin	Control Function	Remark
PB0	77	Information of Sliding cover position	
PB1	76		
PB2	79	External RF output control	
PB3	80		

Baseband A/D Converter Channels usage in N450 and D150

The auxiliary A/D converter channels inside RFI2, N450 are used by MCU to measure battery voltage, charger voltage etc. The A/D converters are accessed by the DSP, D152 via the ASIC, D151. The required resolution is 10 bit. The scaling factor is created using 5% resistors and it is therefore a requirement to have an alignment procedure in the production phase. Each resistor network is supplied with a known input voltage and the measured value is used against the theoretically calculated value. As a result of this operation standard 5% resistors can be used in the voltage scaling circuitry.

The A/D converter used in RFI2, N450 for the measurement are sigma–delta type and the zero value is centered around 50 % of the supply voltage, 1.6V. This means that the A/D converter reading is negative when the input voltage to the converter is less than half of the supply voltage. In calculations the true A/D reading is got by adding 800H to the read value module 4096.

The MCU has 4 10 bit A/D channels which are used in parallel to the channels in N450. The MCU can measure charger voltage, battery size, battery temperature and accessory detection by using it's own converters.

Baseband N450 A/D Converter Channel Usage

Name:	Usage:	Input volt. range	Remark
Chan 0	Battery voltage	5...9 V	Battery voltage when TX is active
Chan 1			
Chan 2			
Chan 3			
Chan 4			
Chan 5	System Board Temp	0...3.2 V	Used to compensate LCD display contrast
Chan 6	REFOUT voltage	0...3.2 V	Reference voltage calibration input
Chan 7	Battery voltage	5...9 V	Battery volt. TX inactive

MCU Baseband A/D Converter Channel Usage

Name:	Usage:	Input volt. range	Remark
Chan 0	Battery temperature	0...3.2 V	
Chan 1	Charger voltage	5...16 V	
Chan 2	Accessory detection	0...3.2 V	
Chan 3	Battery size indicator	0...3.2 V	

Battery Voltage Measurement

The battery voltage is measured using RFI2, N450 A/D converter channel 0 and 7. The converter value supplied from channel 0 is measured when the transmitter is active. This measurement gives the minimum battery voltage. The value from channel 7 is measured when the transmitter is inactive. The battery voltage supplied to the A/D converter input is switched off when the baseband is in power off. The battery voltage measurement voltage is supplied by PSCLD, N300 which performs scaling, the scaling factor is R1(R1+R2), and switch off. The measurement voltage is filtered by a capacitor to achieve an average value that is not depending upon the current consumption behavior of the

baseband. To be able to measure the battery voltage during transmission pulse the time constant must be short. The value for the filtering capacitor is set to 10 nF, C319. The scaling factor used to scale the battery voltage must be 1:3, which means that 9V battery voltage will give 3V A/D converter input voltage. The A/D converter value in decimal can be calculated using the following formula:

$A/D = 1023xR1xU_{BAT}/((R1+R2)xU_{ref}) = 1023xU_{BAT}xK$

where K is the scaling factor. $K = R1/((R1+R2)xU_{ref)}$.

Charger Voltage Measurement

The charger voltage is measured to determine the type of charger used. MCU A/D converter channel 1 is used for this purpose and MCU /D converter channel 1. The input circuitry to the charger measurement A/D channel implements an LP filter. The input voltage must be scaled before it is fed to the A/D converter input. Due to the high input voltage range scaling is performed outside PSCLD, N300. The scaling factor required is 22/(22+100) = 0.18. The charger voltage measurement switch is integrated into PSCLD, N300. Charger voltage is not supplied to the A/D converter input in power off mode. This is done to protect the A/D converter input in case power is switched off and the charger remains connected to the baseband. The resistor values are different since the scaling factor is larger.

Battery Size Resistor Measurement

The battery size, capacity is determined by measuring the voltage on the BSI pin on the battery pack when the battery is attached to the phone. The auxiliary channel 2 is used for this purpose. The BSI signal is pulled up on the base band using a 47 kohm resistor and the resistor inside the battery pack is reflecting the capacity of the battery. There are two special cases to be detected by the MCU. The first case is the Lithium battery. The Lithium battery has reserved values in the battery size table. Lithium type batteries are all the same from charging point of view. Lithium batteries are charged to a constant voltage and charging is aborted when the predefined voltage is reached. The Lithium battery capacity is a function of the battery voltage. The battery voltage drops linearly as the battery is discharged. The other case that has to be handled is the dummy battery. This battery is used for A/D converter field calibration at service centers and together with a defined voltage on the BTEMP pin on the battery pack to put the baseband into Local mode in production. Battery sizes below 143 mAh will be treated as dummy battery. The battery size A/D converter value can be calculated using the following formula:

$A/D = RSI/(RSI+47\ kohm)x1023$

where RSI is the value of the resistor inside the battery pack.

Battery Size and A/D Converter Value

Battery Type	Battery pack resistor	Capacity	BSI volt.	A/D conv value
Dummy	1 kΩ 2 %	<143 mAh	0.07	24 h (36)
Lithium type 1 standard battery	68 kΩ 2 %	400 mAh		25 C (605)
Lithium type 1 extended battery	68 kΩ 2 %	900 mAh		25 C (605)
Lithium type 2	82 kΩ 2 %	400 mAh		28 A (650)

Battery Temperature Measurement

The battery temperature is measured during charging. The BTEMP pin to the battery is pulled up on baseband by a 47 kohm resistor to logic supply voltage, 3.2V. The voltage on the BTEMP pin is a function of the battery pack temperature. Auxiliary A/D channel 3 is used for this purpose. Inside the battery pack there is a 47 kohm NTC resistor to ground. The A/D converter value can be calculated from the following formula:

A/D = RNTC/(RNTC+47 kohm)x1023

where RNTC is the value of the NTC resistor inside the battery pack.

The relationship between different battery temperature, BTEMP voltage and A/D converter values are shown in the table below. Battery temperature is measured from –56 to 76 Centigrade. (9 HEX to 383 HEX)

A/D Converter Values for Different Battery Temperatures

Bat. temp.	NTC value	BTEMP voltage	A/D conv. value
–25	745.60 kΩ	2.96 V	962
0	164.96 kΩ	2.45 V	796
25	47 kΩ	1.58 V	512
50	16.26 kΩ	0.81 V	263
70	7.78 kΩ	0.45 V	145

External Accessory Detection via XMIC/ID –line

Auxiliary A/D channel 4 is used to detect accessories connected to the system connector using the XMIC/ID. To be able to determine which accessory has been connected MCU measures the DC voltage on the XMIC/ID input. The accessory is detected in accordance with the CAP Accessory specifications. The base band has a pull–up resistor network of 32 kohm to VA. The accessory has a pull down. The A/D converter value can be calculated using the following formula:

A/D = (ACCI+10 kohm)/(ACCI+32 kohm)x1023x/3.2 .

where ACCI is the DC input impedance of the accessory device connected to the system connector

The different values for acceptable accessories are given in the following table. The values in the table are calculated using 5 % resistor values and power supply range 3–3.3 V. Due to that the pull up resistor in the XMIC line is divided into two resistors. The voltage at the A/D converter input is different from that on the XMIC.

Accessory Detection Voltage

Acc. type	Acc. resistance	Voltage on A/D converter channel 5 (min/typ/max)	A/D converter value(Dec)
IR Link	100 kΩ	2.43...2.63...2.83	853
Headset	47 kΩ	2.1...2.27...2.40	739
Compact HF	22 kΩ	1.23...1.87...2.03	607

Keyboard Interface

The keypad matrix is located on a UI module Flex PCB and the interface to the base band is by using connector X101. The power on key is also connected to the PSCLD to switch power on. Due to the internal pull up inside PSCLD, N300 to a high voltage, a rectifier, V418 is required in the keypad matrix for the power on keypad to prevent the high voltage to interfere with the keypad matrix.

Series resistors, R261–R264 are implemented in the Column output to reduce the EMI radiation to the UI Flex. Capacitors C257–C260 reduces the EMC radiation and absorbs any ESD produced over an air gap to the keymat. As the serial display driver interface uses ROW5 for data transmission series resistors are needed to prevent keypad or double keypad pressing from interfering with the display communication. In a similar way R265–R269 in the ROW lines reduces the EMI to the UI board. Capacitors C251–C256 implements a LP–filter together with each resistor in the ROW line. The capacitors also absorbs ESD pulses over an air gap to the keymat.

During idle when no keyboard activity is present the MCU sets the column outputs to ”0” and enables the keyboard interrupt. An interrupt is generated when a ROW input is pulled low. Each ROW input on the ASIC, D151 has an internal pull–up. The keyboard interrupt starts up the MCU and the MCU starts the scanning procedure. As there are keypads to be detected outside the matrix the MCU sets all columns to ”1” and reads the ROW inputs if a logic ”0” is read on any ROW this means that one of the 6 possible non matrix keypads has been pressed. If the result was a ”1” on each ROW the MCU writes a ”0” on each column consecutively while the rest of the column outputs are kept in tri–state to allow dual keypad activation to be detected. After that the keyboard scanning is completed and no activity is found the MCU writes ”0” to all columns, enables the keyboard interrupt and enters sleep mode where the clock to the MCU is stopped. A key press will again start up the MCU.

Keyboard and Display Light

The display and keyboard are illuminated by LED's. The light is normally switched on when a keypad is pressed. The rules for light switching are defined in the SW UI specifications. The display and keyboard lights are controlled by the MCU. The LED's are connected two in series to reduce the power consumption. Due to the amount of LED's required for the keyboard and display light they are divided into two groups. Each group has it's own control transistor. The LED switch transistor is connected as a constant current source, which means that the current limiting resistor is put in the emitter circuitry. This arrangement will reduce LED flickering depending upon battery voltage and momentary power consumption of the phone. The LED's are connected straight to the battery voltage. This connection allows two LED's to connected in series. The battery voltage varies a lot depending upon if the battery is charged, full or empty. The switching transistor circuitry is designed to improve this as mentioned earlier.

The light requirement is different for the display and the keyboard. This is one of the reason for splitting the LED control among three transistors. Each LED group can now be set to different LED current thus affecting the illumination. The reason for splitting the LED control is the power dissipation in the control transistor and the current limiting resistor. This is particular the problem during charging when the battery voltage is high.

The LED transistor control lines are coming from PSCLD. The MCU controls these lines by writing to PSCLD using the serial control bus. There are two LED control lines provided by the PSCLD. The display and keyboard light controls are connected to a separate control lines. This means that the keyboard and display light can be controlled separately. The advantage of this is that the power dissipation and heating of the phone can be reduced by only having the required lights switched on.

There is no PWM control on these PSCLD control lines to allow dimming of the keyboard and display lights. These control outputs from PSCLD are low when PSCLD exits reset, lights are off, and MCU then switches them on according to the user settings or user actions.

Audio Control

The audio codec N200 is controlled by the MCU, D150. Digital audio is transferred on the CODECB(5:0). PCM data is clock at 512 kHz from the ASIC and the ASIC also generates 8 kHz synchronization signal for the bus. Data is put out on the bus at the rising edge of the clock and read in at the falling edge. Data from the DSP, D152 to the audio codec, N200 is transmitted as a separate signal from data transmitted from the audio codec, N200 to the DSP, D152. The communication is full duplex synchronous. The transmission is started at the falling edge of the synchronization pulse. 16 bits of data is transmitted after each synchronization pulse.

The 512 kHz clock is generated form 13 MHz using a PLL type of approach which means that the output frequency is not 512 kHz at any moment. The frequency varies as the PLL adjusts the frequency. The average frequency is 512 kHz. The clock is not supplied to the codec when it is not needed. The clock is controlled by both MCU and DSP. DTMF tones are generated by the audio codec and for that purposes the 512 kHz clock is needed. The MCU must switch on the clock before the DTMF generation control data is transmitted on the serial control bus.

The serial control bus uses clock, data and chip select to address the device on the bus. This interface is built in to the ASIC and the MCU writes the destination and data to the ASIC registers. The serial communication is then initiated by the ASIC. Data can be read form the audio codec, N200 via this bus.

Internal Audio

The bias for the internal microphone is generated from the PSCLD, N300 analog output, VA using a bias generator. The bias generation is designed in such a way that common mode signals induced into the microphone capsule wires are suppressed by the input amplifier in the audio codec. The bias generator is controlled by the MCU to save power, the control signal is taken from the audio codec, N200 output latch, pin 26, when the microphone is not used, in idle the bias generator is switched off. The microphone amplifier gain is set by the MCU to match with the used microphone, 35 dB. The microphone amplifier input to the audio codec is a symmetrical input.

The microphone signal is connected to the baseband using filtering to prevent EMC radiation and RF PA signal to interfere with the microphone signal. L201 and C201 forms the first part of this filter in main radio unit. R203 and C202 forms the second part of this filter. A similar filter is used in the negative signal path of the microphone signal. R205 is connected in the ground path for the microphone bias current. R202 supplies the bias current to the microphone from the generator circuitry R201, C200 and V200.

The earpiece amplifier used for the internal earpiece is of differential type and is designed as a bridge amplifier to give the output swing for the required sound pressure. Since the power supply is only 3V a dynamic type ear piece has to be used to achieve the sound pressure. This means that the ear piece is a low impedance type and represents a significant load to the output amplifier. Series inductors are implemented to prevent EMC radiation from the connection on baseband to the earpiece. The same filter also prevents the PA RF field from causing interference in the audio codec, N200 output stage to the earpiece.

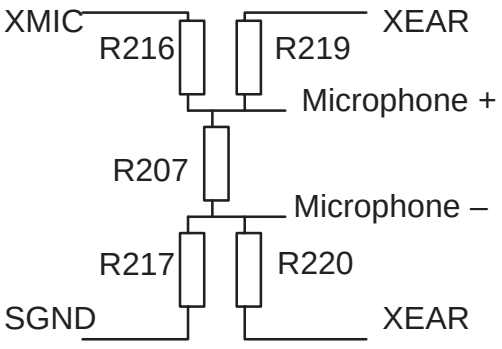
The buzzer is controlled by the PWM output provided by the audio codec, N200. Transistors V425 and V403on the UI flex board acts as amplifier and, impedance conversion for the low impedance buzzer. The buzzer is driven from the battery voltage via the V401 regulator circuit. As the buzzer is connected to the baseband via the keyboard connector, the buzzer driving signal BUZZER is EMC protected. As the buzzer is a dynamic one the impedance shows a clear

inductance. Therefore a free running diode V413 in UI flex is used to clip the voltage spikes induced in the Buzzer line when the buzzer is switched off.

The buzzer frequency is determined by the internal setup of N200. The frequency is determined by the MCU via the serial control bus. The output level can be adjusted by the PWM function which is attached to the buzzer output in N200.

External Audio

The external microphone audio signal is applied to the baseband system connector and connected to the audio block using signals XMIC and SGND. In order to improve the external audio performance the input circuitry is arranged in a sort of dual ended. A wheatstone type of bridge configuration is created by resistors R216, R217, R219 and R220. The signal is attenuated around 20 dB to not cause distortion in the microphone amplifier. The microphone signal is attenuated by resistors R216, R207 and R217. To allow the external earpiece to be driven dual ended the external microphone signal ground is connected to the negative output of the external audio earpiece amplifier. This means that with reference to audio codec, N200 ground there is a signal level on the SGND line. This arrangement requires that the external microphone amplifier supplies the signal on the SGND line to the XMIC line. With this arrangement the differential voltage over R207 caused by the signal in the SGND line is canceled. There is however a common mode component which is relatively high presented at both the external microphone input pins at the audio codec input, pins 31 and 30. The microphone amplifier has a good common mode rejection ratio but a slight phase shift in the signals will remove the balance. To compensate for this the signal from the external earpiece amplifier positive output, which also feeds the external audio output from the baseband is feed to the remaining resistors in the bridge, R219 and R220. This arrangement will attenuate the common mode signal presented to the microphone amplifier caused by the audio signal in the SGND line. Since the positive output from the audio codec, XEAR signal introduces a DC signal to the microphone amplifier the DC signal on the XMIC and SGND lines are blocked by capacitors C218 and C220.



The external audio output is the XEAR signal on the system connector pin. The XEAR signal is taken from audio codec N200 pin 3. The output impedance is increased to nominal 44 ohms by resistors R214 and R214. Theese resistors

prevents the output amplifier from being short circuited even if the pin at the system connector is short circuited. The DC voltage at the XEAR output is used to control the mute function of the accessory. When internal audio is selected the XEAR amplifier in N200 is switched off and the DC voltage at the output on pin 2 is removed. External audio output level is adjusted by the variable gain amplifier in the N200 by MCU via the serial control bus from the ASIC, D151. R118 creates ESD protection for Codec input. L104, C102 and filter creted by R232,C214, C111 and R214 are EMC protection for the XEAR signal at the system connector. This filterering also prevents RF signals induced in the external cables from creating interference in the audio codec output stage.

DSP

The DSP used is the TMS320LC541 .This is 16 bit DSP that can use external and/or internal memory access. The DSP can operate in two modes microprocessor mode or microcontroller mode. The difference between the two modes are that in microprocessor mode the DSP boots from external memory while in the microcontroller mode the DSP boots from internal ROM. The DSP external memory access is devided into data, program and I/O access. The type of access is indicated on three control pins that can be used for memory control.

The DSP, D152 executes code from the internal ROM. The baseband also provides external fast memories for the DSP, D404 and D405. The DSP is capable of addressing 64 kword of memory. The memory area is divided into a code execution area and a data storage area. The code execution area is located at address 8000H–FFFFH. The external memories are arranged in such a way that the DSP can access the external memories both as data storage and code execution. The memory chip select is taken from the memory access strobe signal from the DSP. This means that the memory is active during any memory access. The memories are connected in such a way that the write control is CE controlled write. This means that both the write signal and the output enable signal are active at the same time. This implementation is required since the DSP supports only one signal for write/read control.

The DSP is operating form the 13 MHz clock. In order to get the required performance the frequency is internally increased by a PLL by a factor of 3. The PLL requires a settling time of 50 us after that the clock has been supplied before proper operation is established. This settling counter is inside the DSP although the ASIC, D151 contains a counter that will delay the interrupt with a programmable amount of clock cycles before the interrupt causing the clock to be switched on is presented to the DSP.

The DSP has full control over the clock supplied to it. When the DSP is to enter the sleep mode the clock is switched off by setting a bit in the ASIC register. The clock is automatically switched on when an interrupt is generated.

DSP Interrupts

The DSP supports 4 external interrupts. Three interrupts are used. The ASIC, D151 generates two of the interrupts. One interrupt is generated by RFI2, N450

auxiliary A/D converter. This interrupt is generated when a baseband measurement A/D conversion is completed. The interrupts to the DSP are active low.

DSP Serial Communications Interface

The DSP contains two synchronous serial communications interface. One of the interfaces are used to communicate with the audio codec, N200. The 512 kHz clock required for the data transfer is provided by D151 as well as the 8 kHz synchronization signal. Data is transferred on to lines, RX and TX creating a full duplex connection. Data is presented on the bus on the first rising edge of the clock after the falling edge of the synchronization pulse. Data is read in by each device on the falling edge of clock. Data transfer is 16 bits after each synchronization pulse.

The DSP, D152 has control over the clock provided to the audio codec. The DSP can switch on the clock to start the communication and switch it off when it is not needed. This clock is also under control of MCU, D150 as described in the previous section Audio Control.

The second serial interface is used for debugging and Digital Audio Interface. The ASIC provides the clock and the synchronization for this serial interface as well since the two serial interfaces need to be operated synchronously in case of DAI measurements.

RFI2, N450 Operation

The RFI2, N450 contains the A/D and D/A converters to perform the A/D conversion from the received signal and the D/A converters to perform the conversion for the modulated signal to be supplied to the transmitter section. In addition to this the RFI2 chip also contains the D/A converter for providing AFC voltage to the RF section. This AFC voltage controls the frequency of the 13 MHz VCO which supplies the system clock to the baseband. The RFI2, N450 also contains the D/A converter to control the RF transmitter power control. The power control values are stored in the ASIC, D151 and at the start of each transmission the values are read from the ASIC, D151 to the D/A converter producing the power control pulse. This D/A converter is used during the reception to provide AGC for the receiver RF parts.

One of the A/D converters used for receiver signal conversion can be used as an auxiliary converter that supplies 8 channels for baseband measurement purposes. When the converter is used in this mode each conversion generates an interrupt directly to the DSP. The DSP operates this converter via the ASIC, D151.

Data communication between the ASIC, D151 and RFI2, N450 is carried out on a 12 bit parallel data bus. The ASIC, D151 uses 4 address lines to access RFI2, N450. Depending on the direction of the communication either the write control signal is used to write data to RFI2, N450 or the read signal is used to read data from RFI2, N450. The ASIC, D151 supplies 13 MHz clock to the RFI2, N450. This clock is used as reference for the A/D and D/A converters.

Communication between the ASIC, D151 and the RFI2, N450 is related to the clock.

The RFI2, N450 digital supply is taken from the baseband main digital supply. The analog power supply, 4.5V is generated by a regulator N451 supplied form the VBATT voltage. The analog power supply is always supplied as long as the baseband is powered and VXOENA signal is activated (low).

SIM Interface

The SIM interface is the serial interface between the smart card and the baseband. The SIM interface logic levels are 5V since no 3V technology SIM is yet available. The baseband is designed in such a way that a 3V technology SIM can be used whenever it is available. The SIM interface signals are generated inside the ASIC. The signals coming from the ASIC are converted to 5V levels. The PSCLD circuit is used as the logic voltage conversion circuit for the SIM interface. The PSCLD circuit also contains the voltage regulator for the SIM power supply. The control signals from the ASIC to PSCLD are at 3V level and the signals between PSCLD and the SIM are 5V levels. An additional control line between the ASIC and the PSCLD is used to control the direction of the DATA buffer between the SIM and the PSCLD. In a 3V technology environment this signal is internal to the ASIC only. The pull up resistor required on the SIM DATA line is integrated into the PSCLD and the pull–up is connected to the SIM regulator output inside PSCLD. In idle the DATA line is kept as input by both the SIM and the interface on the base band. The pull–up resistor is keeping the DATA line in it’s high state.

The power up and power down sequences of the SIM interface is performed according to ISO 7816–3. To protect the card from damage when the power supply is removed during power on there is a control signal, CARDDETX, that automatically starts the power down sequence. The CARDDETX information is taken from the battery size indicator signal, BSI, from the battery connector. The battery connector is designed in such a way that the BSI signal contact is disconnected first, while the power is still supplied by the battery, and the battery power contacts are disconnected after that the battery pack has moved a specified distance.

Since the power supply to the SIM is derived from PSCLD also using 3V technology SIM the power supply voltage of the SIM regulator is programmable 3.15/4.8 V. The voltage is selected by using the serial control bus to PSCLD. The default value in PSCLD’s hardware is set to 3.2V nominal.

For cross compatibility reasons the interface is always be started up using 3V. The 3V technology SIM will operate at 5V but a 5V SIM will not always operate at 3V. The supply voltage is switched to 5V if the SIM is needeing that. The SIM has a bit set in a data field indicating it’s capability of 3V or 5V operation.

The DATA signal between the SIM and the PSCLD can be set to operate in two different modes. One mode causes the PSCLD output to force a logic high level on the DATA line when the interface is driving a high level. In this mode the interface output is driving the DATA line actively. In the other mode the DATA line

is operating like an open drain circuitry with the difference that during the transition periods high–low, low–high the interface is actively forcing the DATA line. The advantage of this is that the DATA line is acting like an open drain, tri–state, data line but there is no problem with rise times since the data line is actively forced during the transition period. This mode is introduced to cope with data line overshoots that has been discovered during type approval testing. The present solution is to force the data line actively during the byte transmission. In the new mode the data line is not forced actively when the data to be transmitted is high.

The regulator control signal is derived from the ASIC and this signal controls the operation of the SIM power supply regulator inside PSCLD. To ensure that the powered off ASIC doesn't cause any uncontrolled operations at the SIM interface the PSCLD signals to the SIM are forced low when the PURX signal is active, low. This implementation will ensure that the SIM interface can not be activated by any external signal when PSCLD has PURX active. When PURX goes inactive the control of the interface signals are given back to the ASIC signals controlling PSCLD SIM interface operations.

The clock to the SIM can be switched off if the SIM card allows stopping of the clock. The clock can be stopped either in high or low state, determined by the card data. For cards not allowing the clock to be stopped there is a 1.083 MHz clock frequency that can be used to reduce the power consumption while the clock is running. In this case the VCO must be running all the time. When the clock is stopped and the status of the CARDIN signal changes, battery is removed, the clock to the SIM is restarted inside the ASIC and the SIM power down sequence is performed.

To be able to handle current spikes as specified in the SIM interface specifications the SIM regulator output from PSCLD must have a ceramic capacitor off 100 nF connected between the output and ground close to the SIM interface connector. To be able to cope with the fall time requirements and the disconnected contact measurements in type approval the regulator output must be actively pulled down when the regulator is switched off. This active pull–down must work as long as the external battery is connected and the battery voltage is above the PSCLD reset level.

The SIM power on procedure is controlled by the MCU. The MCU can power up the SIM only if the CARDDETX signal is in the inactive state. Once the power up procedure has been started the ASIC takes care of that the power up procedure is performed according to ISO 7816–3.

The SIM interface uses two clock frequencies 3.25 MHz or 1.625 MHz during SIM communication. A 1.083 MHz clock is used during SIM sleep state if the clock is not allowed to be switched off. The data transfer speed in the SIM GSM session is specified to be the supplied clock frequency/372. The ASIC SIM interface supplies all the required clock frequencies as well as the required clock frequency for the UART used in the SIM interface data transmission/reception.

Display Driver Interface

The display driver is Seiko SD1560, located in UI Flex board. The display driver has internal voltage triple circuitry for LCD voltage generation. Capacitors C409 and C420 are used in the voltage converter. Capacitor C 404 is the filtering capacitor for the voltage generator output. Capacitors C400–C403 and C421 are filtering capacitors for the supply voltage to the display driver back plane voltages. Resistor network R416–419 forms the feedback network for setting the contrast for the display. The display driver has internal temperature compensation for the contrast.

The Base Band uses a serial interface to the Seiko LCD driver. The serial interface is designed in the ASIC. The MCU writes data into the serial interface in the ASIC and it is then transmitted to the LCD driver. The LCD driver reset is controlled by the MCU on P40. The display driver reset is low level active. The P40 pin on the MCU has a pull down capacitor, C154 to ensure that the LCD driver reset is low at power up. After exiting reset one of the first tasks for the MCU is to set the P40 to output and low, ”0”. After at least 100 us the reset signal to the display driver is taken high, ”1”. This rising edge reset selects 80XX type MCU interface. The serial interface setting of the driver will override this. After resetting the display driver the MCU starts the initialization procedure using the serial interface in the ASIC, D151.

The MCU first sets up the display driver interface in the ASIC for the serial driver. This enables the interface signals and sets the polarity of the chip select to the driver correct. The next step is to blank the display. This is to be done soon after the power up sequence to ensure that no garbage is output on the display. The normal display test pattern is then written to the display.

Communication with the serial driver takes place on the SCONB(5:0). The display driver requires serial data, serial clock and command/display information during the serial transfer. The display driver has its own chip select which is active during the transfer, there are other devices on the same serial bus as well. The command/display information is transmitted on the keyboard ROW5 output. Due to the fact that the keyboard interface is used during display driver transfers the keyboard activities must be disabled during display driver communication. This means that the column output from the ASIC must be put in high impedance state not to interfere with the data transmission if keypads are pressed.

The timing required for the serial interface is provided by the ASIC and the operation of ROW5 depends upon the display driver interface initialization. For the serial interface it is used for command/display data control. The serial clock is 1.083 MHz.

The serial interface in the ASIC starts the transfer after each write operation to the output buffer. The data transferred is command or data depending upon to which address it is written in the interface. The ASIC sets the control signal on ROW5 accordingly. After that the data has been shifted out from the interface a bit is set in the interface register to tell the MCU that the interface is ready for

the next byte. This transmission indicator bit is polled by the MCU and the next byte is written when the output buffer is empty.

The clock to the display driver interface in the ASIC is automatically switched on when a write operation to the interface has taken place. The MCU can force the clock to be continuously on by writing the clock on to the CTSI block. The default assumption is that the MCU forces the clock to be continuously on only when a large amount of data is to be transmitted, such as segment test at power up.

RF Block

Introduction

The GJ8A is the RF module of the NHE–6 cellular transceiver (phase 2). The GJ8A module carries out all the RF and system functions of the transceiver. This module works in the GSM system.

The GJ8A module is constructed on a 1.0 mm thick FR4 eight–layer printed wiring board. The dimensions of the PWB are 126 mm x 43 mm.

Components are located on both sides of the PWB. The RF components are located on the top end of the PWB. The both sides of the board includes high and low components. The maximum usable height is 5 mm.

EMI leakage is prevented by a metallized plastic shield A on side 1/8 and a metallized plastic cover B on side 8/8. The shield A also conducts the heat out of the inner parts of the phone, thus preventing excessive temperature rise.

Receiver

The SW controlled electrical switch connects the signal from the antenna (transceiver antenna or external) to the duplex filter, which rejects the unwanted signals. The received signal is amplified by a discrete low noise preamplifier. The gain of the amplifier is controlled by the AGC control line (PDATA0). The nominal gain of 20 dB is reduced in strong field conditions by about 40 dB. After the preamplifier the signal is filtered by the SAW RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the receiver unit.

The filtered signal is down converted by the single balanced diode mixer. The first IF is 71 MHz. The first local signal is generated by the UHF synthesizer.

The amplified IF signal is filtered by the SAW IF filter. The filter rejects the adjacent channel signal, intermodulating signals and the second IF image signal. After filtering, the IF signal is fed to the receiver ASIC (CRFRT), which includes the AGC amplifier and the 2nd mixer. The 2nd local signal is generated in the RF ASIC by dividing the VHF signal by four. After mixing the 2nd IF signal is filtered by the SMD 13 MHz ceramic filter and amplified by the differential amplifier of the ASIC. The differential 13 MHz signal is fed through the attenuator circuit to the RF interface circuit RFI2.

Duplex Filter

The duplex filter combines the transmitter and the receiver to the antenna connection. The TX filter rejects the noise power at the RX frequency band and TX harmonic signals. The RX filter rejects blocking and spurious signals coming from the antenna. It protects the receiver of the transmitter power, too.

Pre–Amplifier

The pre–amplifier amplifies the received signal. The performance of the amplifier determines the sensitivity of the receiver.

Parameter	*Value*
Frequency band:	*935–960 Mhz*
Supply voltage (min/max):	*4.5...4.8 V*
Current consumption (typ):	*10 mA*
Insertion gain (min/typ):	*15...20 dB*
Noise figure (max):	*2.0 dB*
Reverse isolation (min):	*15 dB*
Gain reduction (typ):	*40 dB*
IIP3: (min):	*–10 dBm*
Input VSWR; zo=50 Ω (max):	*2.0*
Output VSWR; zo=50 Ω (max):	*2.0*

RF Interstage Filter

The RX interstage filter is an SAW filter. The filter rejects spurious and blocking signals coming from the antenna. It rejects the local oscillator signal leakage, too.

Diode Mixer

The first mixer is a single balanced diode mixer. The mixer consists of a microstripline balun and a ring quad schottky diode. One diode pair is used for the receiver and the other is used for up conversion of the transmitter signal.

Parameter	*Value*
RX frequency range:	*935–960 Mhz*
LO frequency range:	*1006–1031 Mhz*
IF frequency:	*71 Mhz*
Conversion loss (typ/max):	*7...9 dB*
IIP3 (typ):	*5 dBm*
LO – RF isolation (min):	*15.0 dB*
LO power level (max):	*3 dBm*

IF Amplifier

The first IF bipolar transistor amplifier drives up the level of the down converted signal before filtering.

Parameter	*Value*
Operation frequency:	*71 Mhz*
Supply voltage (min/max):	*4.5...4.8 V*
Current consumption (typ):	*18 mA*
Insertion gain (min/typ):	*19...20 dB*
Noise figure (typ):	*3.0 dB*
IIP3 (min):	*–5 dBm*

First IF Filter

The first IF filter makes the part of the channel selectivity of the receiver. It rejects adjacent channel signals (except the 2nd adjacent). It also rejects blocking signals and the 2nd image frequency.

The first IF amplifier is a bipolar transistor amplifier.

Parameter	*Value*
Center frequency:	*71 Mhz*
Operating temperature range	*–20...+80 °C*
Input impedance:	*3.5 kΩ//6.9 pF*
Output impedance:	*3.4 kΩ//6.7 pF*
Insertion loss (typ/max):	*11.5...13.5 dB*
Group delay distortion:	*700...1300 ns*
2 dB bandwidth (min):	± *80 kHz*
3 dB bandwidth (min):	± *120 kHz*
5 dB bandwidth (max):	± *230 kHz*
20 dB bandwidth (max):	± *400 kHz*
30 dB bandwidth (max):	± *600 kHz*
35 dB bandwidth (max):	± *800 kHz*
Spurious rejection at fo ±26 MHz (min):	*60 dB*

Receiver IF Circuit, RX part of CRFRT

The receiver part of CRFRT consists of an AGC amplifier, a mixer and a buffer amplifier for the second IF. The mixer circuit down converts the received signal to the 13 MHz IF frequency. After second IF filter the signal is amplified and fed to baseband circuitry. The supply current can be switched OFF by an external switch.

Parameter	*Value*
Supply voltage (min/typ/max):	*4.27...4.5...4.73 V*
Supply current (typ):	*38 mA*
Input frequency range (min/max):	*45...87 MHz*
Max voltage gain before 2IF filt:	*47 dB*
Min voltage gain before 2IF filt:	*–10 dB*
AGC gain control slope (min/typ/max):	*40...84...120 dB/V*
Absolute gain inaccuracy (min/max):	*–4...4 dB*
Relative gain inaccuracy (max):	*0.8 dB*
Noise figure (max):	*15 max gain*
Mixer output 1 dB comp point (typ):	*1.0 V_{PP}*
Gain of the 2nd IF buffer:	*30*
Max output level after 2nd IF buffer (typ):	*1.6 V_{PP}*

Second IF Filter

The second IF is filtered by the ceramic filter, which makes the part of the channel selectivity of the receiver.

Parameter	*Value*
Center frequency (typ):	*13.0 MHz*
1 dB bandwidth BW (min):	*± 90 kHz*
5 dB bandwidth (max):	*± 220 kHz*
Insertion loss (max):	*6.0 dB*
Group delay distortion (max):	*1500 ns at BW*
Attenuation fo±400 kHz (min/typ):	*25.0...30 dB*
Attenuation fo±600 kHz (min/typ):	*40.0...45 dB*
Terminating impedance (typ):	*330 Ω*
Operating temperature range (min/max):	*–30...+85 °C*

Transmitter

The synthesized 232 MHz signal is divided by two in the I/Q modulator of the CRFRT. The TX I and Q signals are generated in the RFI2 interface circuit and they are fed differentially to the modulator. The modulated TX IF signal (116 MHz) is amplified by an AGC amplifier. In this application the gain has been set to the maximum level, because the power control has been implemented by the power amplifier.

The TX signal is generated by mixing the UHF VCO signal and the modulated TX IF signal. After mixing the slightly filtered TX signal is amplified by the MMIC amplifier to the level of +5 dBm. The unwanted signals are filtered by the SAW RF filter.

The power amplifier MMIC amplifies the TX signal to the used power level. The maximum output level of the amplifier is 35 dBm, typically.

The power control loop controls the output level of the MMIC power amplifier. The power detector consists of a directional coupler and a diode rectifier. The difference of the power control signal (TXC) and the detected voltage is amplified and used as a control voltage for the power amplifier.

The duplex filter rejects the noise on the receiver band and the harmonic products of the TX signals. The electrical switch connects the signal to the used antenna.

Modulator Circuit, TX part of CRFRT

The modulator of the CRFRT is a quadrature modulator. The input local signal (232 MHz) is divided by two to get accurate 90 degrees phase shifted signals for the I/Q mixer. After mixing the signals are combined and amplified. The output of the IC is single ended and the level is controllable. The maximum output level is 0 dBm, typically.

Parameter	*Value*
Supply voltage (min/max):	*4.27...4.73 V*
Supply current (typ):	*38 mA*

Transmit frequency input	*Value*
LO input frequency (min/max):	*170...400 MHz*
LO input power level (min/typ/max):	*–20...–10...0 dBm*
LO input impedance (min/typ/max):	*70...100...130* Ω

Modulator Inputs (I/Q):	*Value*
Input bias current, balanced (max):	*100 nA*
External DC reference (min/max):	*2.1...2.6 V*
Differential input swing (min/typ/max):	*0.5...0.8...1.1 V_{pp}*
Differential input offset volt. (min/typ/max):	*0...1.0...3.0 mV*
Input impedance (min):	*200 kΩ*
Gain unbalance (min/max):	*–0.5...0.5 dB*

Modulator Output:	*Value*
Available RF power (min/max):	*–45...0, ZiL=50 kΩ*
Suppression of 3rd order prods (max):	*–35 dB*
Carrier suppression (min):	*35 dB*
Noise floor at saturated Pout (max):	*–125 dBm/Hz*

Upconversion Mixer

The mixer is a single balanced diode mixer. The mixer circuit is the same as used in the receiver. The input signal is a modulated 116 MHz signal coming from the quadrature modulator (part of the CRFRT circuit). The TX signal is filtered by using a microstripline trap for the LO signal before amplification.

Parameter:	*Value*
Input frequency (typ):	*116 MHz*
LO frequency range:	*1006...1031 MHz*
TX frequency (min/max):	*890...915 MHz*
Conversion loss (typ/max):	*7.0...8.0 dB*
IIP3 (min):	*–5.0 dBm*
LO – RF isolation (min):	*20 dB*
LO power level (max):	*3.0 dBm*

TX amplifier

The TX amplifier is a bipolar MMIC amplifier. It amplifies the up converted TX signal to the level required by the power amplifier.

Parameter:	*Value*
Operation frequency range:	*890...915 MHz*
Supply voltage (typ):	*4.5 V*
Current consumption (typ):	*20.0 mA*
Insertion gain (min):	*20 dB*
Output power (typ):	*5.0 dBm*
Noise figure (typ):	*4.0 dB*
Input VSWR (Zo=50 Ω) (max):	*2.0*
Output VSWR (Zo=50 Ω) (max):	*2.0*

TX Interstage Filters

The TX filter rejects the spurious signals generated in the up conversion mixer. It rejects the local and IF signal leakages and broad band noise, too.

Parameter:	*Value*
Terminating impedance:	*50 Ω*
Operating temperature range (min/max):	*–25...+80 °C*
Center frequency (fo) (nom):	*902.5 MHz*
Bandwidth (BW) (min):	*± 12.5 MHz*
Insertion loss at BW (max):	*4.0 dBm*
Ripple at BW (max):	*1.0 dB*
Attenuation DC...845 MHz (min):	*30.0 dB*
Attenuation 845...870 MHz (min):	*20.0 dB*
Attenuation 935...980 MHz (min):	*18.0 dB*
Attenuation 980...1500 MHz (min):	*30.0 dB*
Attenuation 1500...3500 MHz (min):	*15.0 dB*

Power Amplifier

The power amplifier is an integrated 3 stage GaAs MMIC. The device amplifies the TX signal to the desired output level. It has been specified for 6,0 volt operation. The power amplifier includes the negative bias generator for the GaAs FETs.

Parameter:	*Value*
Operating frequency range:	*890...915 MHz*
DC supply voltage Vdd (typ):	*6.0 V*
Current consumption Id (nom):	*.1.0 A*
Output power (min):	*35.0 dBm normal cond.*
Output power (typ):	*34.0 dBm, extreme cond.*
Output power control range (min/max):	*60...80 dB*
Input power (min/typ/max):	*0...1.0...10 dBm*
Efficiency (Po=34.5 dBm) (min/typ):	*45...50 %*
Input VSWR (Zo=50 Ω) (typ):	*2.0*
Noise power (in 30 kHz band, 20 kHz above fo) (typ):	*–90.0 dBm*
Stability, Vdd=6.0 V:	*VSWR 6:1*
Operating case temp. range (min/max):	*–20...+90 °C*

Power control circuit

The power control loop consists of a power detector, a differential amplifier (part of CRFRT) and a buffer amplifier. The power detector is a combination of a directional coupler and a diode rectifier. The difference of the power control signal (TXC) and the detected signal is amplified and used for the output power control.

Parameter:	*Value*
Supply voltage (min/typ/max):	*4.5...4.7...4.9 V*
Supply current (typ):	*15 mA*
Power control range (min):	*20/28 dB, phase I / phase II*
Power control inaccuracy (max):	*±1 dB*
Dynamic range (min):	*60 dB*
Input control voltage range (min/max):	*0.6...3.5 V*
Output control voltage range (min/max):	*1.0...4.0 V*

Frequency Synthesizers

The stable frequency source for the synthesizers and baseband circuits is the voltage controlled temperature compensated crystal oscillator, VCTCXO. The frequency of the VCTCXO is 13 MHz. The frequency of the oscillator is controlled by an AFC voltage, which is generated by the baseband circuits.

The operating frequency range of the UHF synthesizer is from 1006 to 1031 MHz. The UHF signal source is the VCO module. The UHF PLL locks the signal for the accurate frequency and it is used as the down conversion signal for the receiver and the up conversion signal for the transmitter.

The operating frequency of the VHF synthesizer is 232 MHz. This signal is fed to the RF ASIC (CRFRT), where it is used for the I/Q modulation and for the down conversion of the first IF. This 232 MHz signal is divided by four inside the CRFRT before using it as a local signal for the mixer.

VCTCXO

The VCTCXO is a module operating at 13 MHz. The 13 MHz signal is used as a reference frequency of the synthesizers and as a clock frequency for the base band circuits.

Parameter:	*Value*
Operating temperature range (min/max):	*–25...+75°C*
Supply voltage (min/max):	*4.5...4.9 V*
Supply current (max):	*2.0 mA*
Output frequency (typ):	*13 MHz*
Output level (typ):	*1.0 Vpp*
Harmonics (max):	*–3 dBc*
Load (typ):	*10//10 kΩ // pF*
Nominal voltage for center freq. (typ):	*2.1 V*
Frequency control (min/max):	*± 18...±30 ppm*
Control sensitivity (max):	*± 20 ppm/V*

VHF PLL

The VHF PLL consists of the VHF VCO, PLL integrated circuit and loop filter. The output signal is used for the 2nd mixer of the receiver and for the I/Q modulator of the transmitter.

Parameter:	*Value*
Start up setting time (max):	*2 ms*
Phase error (max):	*1 deg., rms*
Sidebands (max)	
• ±1 MHz:	*–70 dBc*
• ±2 MHz:	*–80 dBc*
• ±3 MHz:	*–80 dBc*
• >4 MHz:	*–90 dBc*

VHF VCO + Buffer

The VHF VCO uses a bipolar transistor as an active element and a combination of a chip coil and varactor diode as a resonance circuit. The buffer is combined into the VCO circuit so that they use same supply current.

Parameter:	*Value*
Supply voltage (min/typ/max):	*4.3...4.5...4.7 V*
Control voltage (min/typ/max):	*0.7...2.2...3.8 V*
Supply current (typ/max):	*6.0...8.0 mA*
Operation frequency (typ):	*232 MHz*
Output power level (typ):	*3.0 dBm*
Control voltage sensitivity (min/max):	*8.0...14.0 MHz/V*
Phase noise (max)	
• fo ±600 kHz	*–123 dB*
• fo ±1600 kHz	*–133 dB*
• fo ±3000 kHz	*–143 dB*
Pulling figure (min):	*±1.0 MHz*
Pushing figure (max):	*±1.0 MHz*
Frequency stability (max):	*±3.0 MHz, over temp range –10...+75 °C*
Harmonics (max):	*–5 dBc*
Spurious (max):	*–6 dBc*

UHF PLL

The UHF PLL consists of an UHF VCO module, PLL circuit and a loop filter. This circuit generates the LO signal for the down and the up conversion.

Parameter:	*Value*
Start up setting time (max):	*2 ms*
Settling time ±83 MHz (typ/max):	*600...800 µs*
Phase error (typ/max):	*1.5...3.0 deg, rms*
Sidebands (typ/max)	
• ±200 kHz:	*–53...–40 dB*
• ±400 kHz:	*–63...–50 dB*
• ±600 kHz...1.4 MHz:	*<–69...–66 dB*
• 1.4...3.0 MHz:	*max –76 dB*
• >3.0 MHz:	*max –86 dB*

UHF VCO

The UHF VCO is a module which includes an output amplifier, too.

Parameter:	*Value*
Supply voltage (min/typ/max):	*4.1...4.5...4.9 V*
Control voltage (min/max):	*0.7...3.8 V*
Supply current (typ/max):	*7.5...10.0 mA*
Operation frequency range (min/max):	*1006...1031 MHz*
Output power level (min/max):	*–3.0...3.0 dBm*
Control voltage sensitivity (min/typ/max):	*10.0...13.0...16.0 MHz/V*
Phase noise (typ/max)	
• fo ±600 kHz:	*<–135...–120 dBc/Hz*
• fo ±1600 kHz:	*–130 dBc/Hz*
• fo ±3000 kHz:	*–140 dBc/Hz*
Pulling figure (max):	*±1.0 MHz*
Pushing figure (max):	*±1.0 MHz/V*
Frequency stability (max):	*±3.0 MHz, over temp range –10...+75 °C*
Harmonics (max):	*–15 dBc*
Spurious (max):	*–65 dBc*

UHF VCO Buffer

The buffer amplifies the UHF VCO signal. The output signal is used as the LO signal for the single balanced diode mixer used in the down and up conversion.

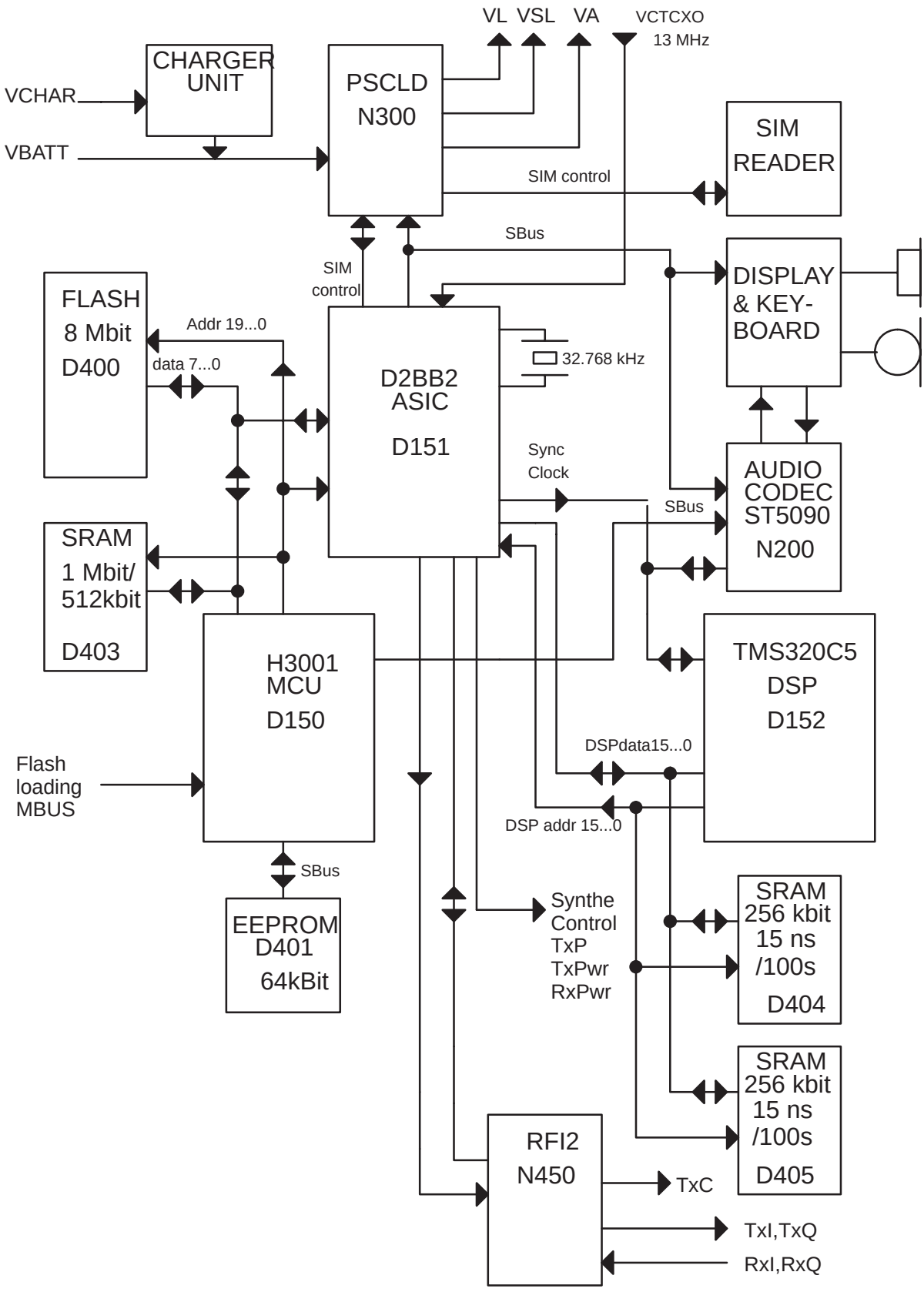
Parameter:	*Value*
Supply voltage (typ):	*4.5 V*
Supply current (typ):	*7.0 mA*
Frequency range (min/max):	*1006...1031 MHz*
Input power (typ):	*–7.0 dBm*
Output power (typ):	*+4.0 dBm*
Harmonics (max):	*–10 dBc*

PLL Circuit

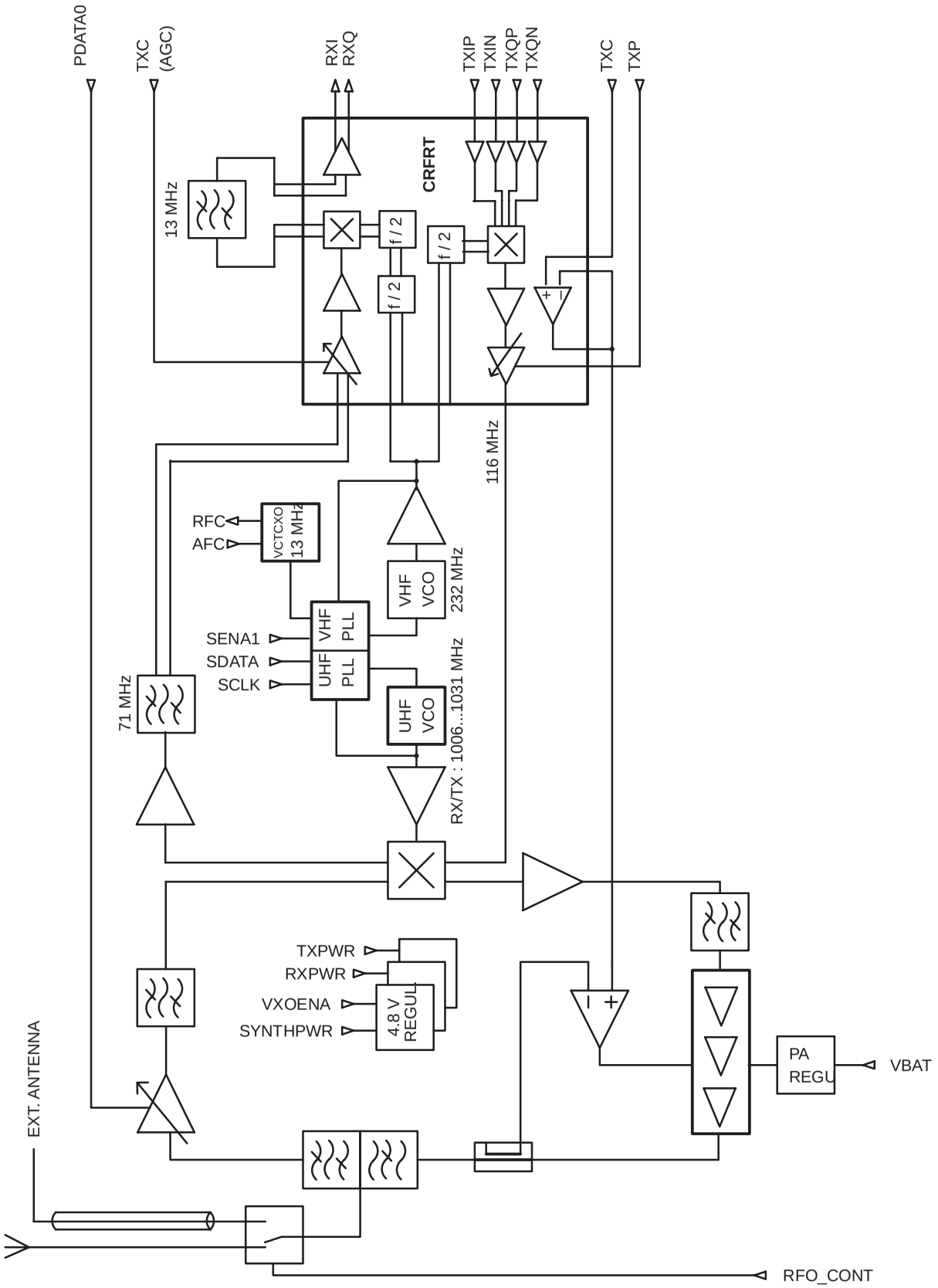
The PLL is National LMX2332. The circuit is a dual frequency synthesizer including both the UHF and VHF synthesizers.

Parameter:	*Value*
Supply voltage (min/max):	*2.7...5.5 V*
Supply current principal synth. (typ):	*8.0 mA*
Supply current auxiliary synth. (typ):	*3.0 mA*
Principal input frequency (min/max):	*100...1200 MHz*
Auxiliary input frequency (min/max):	*50...510 MHz*
Input reference frequency (max):	*40 MHz*
Clocking frequency (max):	*10.0 MHz*
Reference input voltage (min):	*500 mVpp*
Input signal voltage principal s. (min/max):	*–15...+4.0 dBm*
Input signal voltage auxiliary s. (min/max):	*–10...+4.0 dBm*
Phase detector output current tolerance (min/max):	*–20...+20 %*
Phase detector output voltage (min/max):	*0.4 V...Vdd–0.4 V*

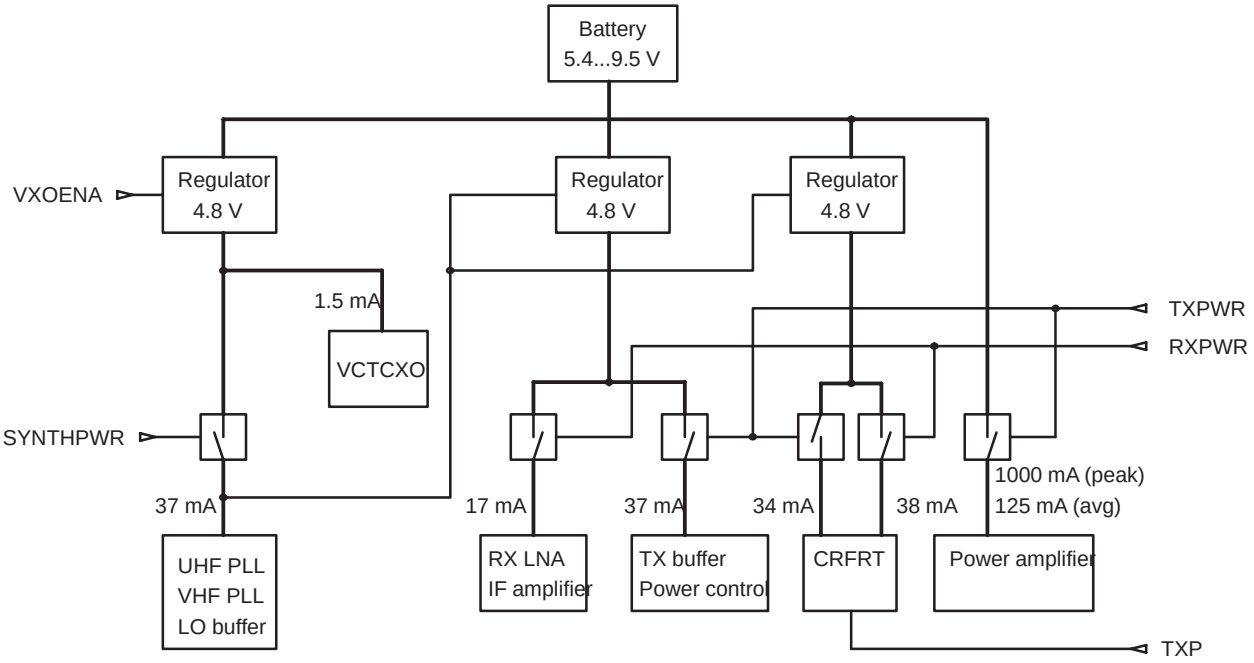
Interconnection Diagram of Baseband



Block Diagram of RF



Power Distribution Diagram of RF



GJ8: Block Diagram of Baseband

GJ8: Circuit Diagram of Power Supply & Charging

GJ8: Circuit Diagram of Central Processing Unit

GJ8: Circuit Diagram of MCU Memory Block

GJ8: Circuit Diagram of Keyboard & Display Interface

GJ8: Circuit Diagram of Audio

GJ8: Circuit Diagram of DSP Memory Block

GJ8: Circuit Diagram of RFI

GJ8: Circuit Diagram of Receiver

GJ8: Circuit Diagram of Transceiver

GJ8: Circuit Diagram of System Connector

Layout Diagrams of GJ8 (Version: 15)

GJ8A: Block Diagram of Baseband

GJ8A: Circuit Diagram of Power Supply & Charging

GJ8A: Circuit Diagram of Central Processing Unit

GJ8A: Circuit Diagram of MCU Memory Block

GJ8A: Circuit Diagram of Keyboard & Display Interface

GJ8A: Circuit Diagram of Audio

GJ8A: Circuit Diagram of DSP Memory Block

GJ8A: Circuit Diagram of RFI

GJ8A: Circuit Diagram of Receiver

GJ8A: Circuit Diagram of Transceiver

GJ8A: Circuit Diagram of System Connector

Layout Diagrams of GJ8A (Version: 02)

Parts list of GJ8 (EDMS Issue 8.8 Code: 0200591 for layout version 15)

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R103	1430001	Chip resistor	100	5 % 0.063 W 0603
R106	1430009	Chip resistor	220	5 % 0.063 W 0603
R308	1430027	Chip resistor	2.43 k	1 % 0.063 W 0603
R309	1430027	Chip resistor	2.43 k	1 % 0.063 W 0603
R216	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R217	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R219	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R220	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R112	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R745	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R746	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R525	1430700	Chip resistor	10	5 % 0.063 W 0402
R558	1430700	Chip resistor	10	5 % 0.063 W 0402
R713	1430700	Chip resistor	10	5 % 0.063 W 0402
R740	1430700	Chip resistor	10	5 % 0.063 W 0402
R506	1430710	Chip resistor	22	5 % 0.063 W 0402
R514	1430710	Chip resistor	22	5 % 0.063 W 0402
R541	1430710	Chip resistor	22	5 % 0.063 W 0402
R595	1430710	Chip resistor	22	5 % 0.063 W 0402
R743	1430710	Chip resistor	22	5 % 0.063 W 0402
R829	1430710	Chip resistor	22	5 % 0.063 W 0402
R831	1430710	Chip resistor	22	5 % 0.063 W 0402
R832	1430710	Chip resistor	22	5 % 0.063 W 0402
R845	1430710	Chip resistor	22	5 % 0.063 W 0402
R847	1430710	Chip resistor	22	5 % 0.063 W 0402
R331	1430714	Chip resistor	33	5 % 0.063 W 0402
R332	1430714	Chip resistor	33	5 % 0.063 W 0402
R151	1430718	Chip resistor	47	5 % 0.063 W 0402
R152	1430718	Chip resistor	47	5 % 0.063 W 0402
R214	1430718	Chip resistor	47	5 % 0.063 W 0402
R218	1430718	Chip resistor	47	5 % 0.063 W 0402
R221	1430718	Chip resistor	47	5 % 0.063 W 0402
R222	1430718	Chip resistor	47	5 % 0.063 W 0402
R324	1430718	Chip resistor	47	5 % 0.063 W 0402
R327	1430718	Chip resistor	47	5 % 0.063 W 0402
R342	1430718	Chip resistor	47	5 % 0.063 W 0402
R453	1430718	Chip resistor	47	5 % 0.063 W 0402
R703	1430718	Chip resistor	47	5 % 0.063 W 0402
R744	1430718	Chip resistor	47	5 % 0.063 W 0402
R115	1430726	Chip resistor	100	5 % 0.063 W 0402
R203	1430726	Chip resistor	100	5 % 0.063 W 0402
R204	1430726	Chip resistor	100	5 % 0.063 W 0402
R305	1430726	Chip resistor	100	5 % 0.063 W 0402

R306	1430726	Chip resistor	100	5 % 0.063 W 0402
R322	1430726	Chip resistor	100	5 % 0.063 W 0402
R323	1430726	Chip resistor	100	5 % 0.063 W 0402
R510	1430726	Chip resistor	100	5 % 0.063 W 0402
R524	1430726	Chip resistor	100	5 % 0.063 W 0402
R570	1430726	Chip resistor	100	5 % 0.063 W 0402
R701	1430726	Chip resistor	100	5 % 0.063 W 0402
R702	1430726	Chip resistor	100	5 % 0.063 W 0402
R784	1430726	Chip resistor	100	5 % 0.063 W 0402
R741	1430726	Chip resistor	100	5 % 0.063 W 0402
R503	1430732	Chip resistor	180	5 % 0.063 W 0402
R742	1430732	Chip resistor	180	5 % 0.063 W 0402
R801	1430732	Chip resistor	180	5 % 0.063 W 0402
R107	1430734	Chip resistor	220	5 % 0.063 W 0402
R502	1430734	Chip resistor	220	5 % 0.063 W 0402
R513	1430734	Chip resistor	220	5 % 0.063 W 0402
R564	1430734	Chip resistor	220	5 % 0.063 W 0402
R568	1430734	Chip resistor	220	5 % 0.063 W 0402
R574	1430734	Chip resistor	220	5 % 0.063 W 0402
R596	1430734	Chip resistor	220	5 % 0.063 W 0402
R781	1430734	Chip resistor	220	5 % 0.063 W 0402
R808	1430734	Chip resistor	220	5 % 0.063 W 0402
R844	1430734	Chip resistor	220	5 % 0.063 W 0402
R559	1430738	Chip resistor	270	5 % 0.063 W 0402
R594	1430738	Chip resistor	270	5 % 0.063 W 0402
R598	1430738	Chip resistor	270	5 % 0.063 W 0402
R557	1430740	Chip resistor	330	5 % 0.063 W 0402
R329	1430744	Chip resistor	470	5 % 0.063 W 0402
R343	1430744	Chip resistor	470	5 % 0.063 W 0402
R547	1430744	Chip resistor	470	5 % 0.063 W 0402
R782	1430746	Chip resistor	560	5 % 0.063 W 0402
R101	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R109	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R150	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R202	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R205	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R261	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R262	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R263	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R264	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R270	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R300	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R301	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R304	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R312	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R314	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R326	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R330	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R560	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R562	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R563	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R792	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R834	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R840	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R780	1430756	Chip resistor	1.2 k	5 % 0.063 W 0402
R565	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R783	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R785	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R200	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R207	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R260	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R265	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R266	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R267	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R268	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R269	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R452	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R521	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R522	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R571	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R586	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R609	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R714	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R717	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R795	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R830	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R843	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R523	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R718	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R790	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R794	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R797	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R587	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R584	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R720	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R820	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R821	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R105	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R501	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R511	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R605	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R608	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R791	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R823	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R824	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R825	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402

R841	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R842	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R551	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R553	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R554	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R556	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R715	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R800	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R583	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R588	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R102	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R104	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R111	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R206	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R208	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R315	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R316	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R317	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R318	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R321	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R458	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R500	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R504	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R505	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R552	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R555	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R573	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R591	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R592	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R597	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R601	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R602	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R604	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R606	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R611	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R712	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R833	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R827	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R828	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R719	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R215	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R303	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R576	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R578	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R580	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R822	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R113	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R572	1430792	Chip resistor	33 k	5 % 0.063 W 0402

R577	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R311	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R313	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R589	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R716	1430800	Chip resistor	68 k	5 % 0.063 W 0402
R114	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R155	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R201	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R302	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R400	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R401	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R402	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R403	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R404	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R405	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R406	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R407	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R408	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R409	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R410	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R411	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R412	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R413	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R414	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R507	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R508	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R603	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R607	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R610	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R612	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R613	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R614	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R456	1430820	Chip resistor	470 k	5 % 0.063 W 0402
R319	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R328	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R512	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R585	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R457	1800659	NTC resistor	47 k	10 % 0.12 W 0805
R116	1825001	Chip varistor vwm18v vc40v	0603	0603
R117	1825001	Chip varistor vwm18v vc40v	0603	0603
R118	1825001	Chip varistor vwm18v vc40v	0603	0603
R725	1825003	Chip varistor vwm5.5v vc15.5	0805	0805
V100	1825007	Chip varistor vwm18v vc39v	1210	1210
C304	2309570	Ceramic cap.		Y5 V 1206
C331	2309570	Ceramic cap.		Y5 V 1206
C821	2310209	Ceramic cap.	2.2 n	5 % 50 V 1206
C823	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C317	2310784	Ceramic cap.	100 n	10 % 25 V 0805

C332	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C336	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C450	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C452	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C743	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C746	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C732	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C745	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C225	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C308	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C309	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C335	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C203	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C206	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C219	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C337	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C572	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C210	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C211	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C710	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C840	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C500	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C513	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C502	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C506	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C518	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C713	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C721	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C847	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C722	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C825	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C712	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C826	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C862	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C591	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C850	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C520	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C718	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C846	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C158	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C159	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C551	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C851	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C107	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C112	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C201	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C204	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C221	2320546	Ceramic cap.	27 p	5 % 50 V 0402

C223	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C229	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C302	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C314	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C338	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C339	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C505	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C514	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C522	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C590	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C593	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C595	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C711	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C714	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C719	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C723	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C724	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C728	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C742	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C780	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C781	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C782	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C783	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C843	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C845	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C863	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C563	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C564	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C102	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C103	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C104	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C106	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C108	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C152	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C154	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C157	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C162	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C165	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C169	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C170	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C207	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C212	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C215	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C216	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C226	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C250	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C251	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C252	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C253	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C254	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C255	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C256	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C257	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C258	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C259	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C260	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C313	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C460	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C503	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C504	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C516	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C523	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C552	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C553	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C554	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C555	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C557	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C558	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C561	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C716	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C717	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C822	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C824	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C830	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C833	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C545	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C546	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C574	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C791	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C213	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C217	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C573	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C844	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C101	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C151	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C156	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C161	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C164	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C166	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C167	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C168	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C303	2320620	Ceramic cap.	10 n	5 % 16 V 0402

C306	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C310	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C311	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C315	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C318	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C321	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C323	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C325	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C326	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C333	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C400	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C401	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C402	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C403	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C404	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C405	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C406	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C407	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C454	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C459	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C105	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C153	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C227	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C228	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C301	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C319	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C330	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C517	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C526	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C562	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C568	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C715	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C741	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C744	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C809	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C834	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C849	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C457	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C556	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C559	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C560	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C602	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C603	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C608	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C110	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C111	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C202	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C205	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402

C515	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C525	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C541	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C569	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C570	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C571	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C740	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C784	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C829	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C832	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C854	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C800	2604079	Tantalum cap.	0.22 u	20 % 35 V 3.2x1.6x1.6
C729	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C601	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C604	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C605	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C320	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C322	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C324	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C300	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C305	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C160	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C200	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C208	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C218	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C220	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C307	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C316	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C329	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C458	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C806	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C841	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C730	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C731	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C734	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C150	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C155	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C163	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C456	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C828	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C831	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
L523	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L524	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L311	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L312	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L102	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L103	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L104	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603

L105	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L106	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L150	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L152	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L153	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L201	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L202	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L203	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L204	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L205	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L306	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L451	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L100	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L101	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L107	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L108	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L300	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L712	3641262	Ferrite bead 30r/100mhz 2a	1206	1206
L800	3641324	Chip coil	10 u	10 % Q=25/2.52 MHz 1008
L711	3643003	Chip coil	12 n	5 % Q=30/250 MHz 0805
L551	3643021	Chip coil	47 n	5 % Q=40/200 MHz 0805
L841	3643021	Chip coil	47 n	5 % Q=40/200 MHz 0805
L520	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L709	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L710	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L840	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L521	3643037	Chip coil	180 n	5 % Q=35/100 MHz 0805
L545	3643037	Chip coil	180 n	5 % Q=35/100 MHz 0805
L522	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L543	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L544	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
V780	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V842	4110018	Cap. diode	BB135	30 V SOD323
V511	4110083	Schdix4 bat15–099r ring	sot143	SOT143
V301	4110130	Zener diode	BZX84	2 % 5.1 V 0.3 W SOT23
V592	4112464	Pindix2 bar64–04 200v 0.1a	sot23	SOT23
V305	4115804	Schottky diode	PRLL5817	20 V 1 A SOD87
V200	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V302	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V303	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V309	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V311	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V608	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V830	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V512	4210011	Transistor	BFS505	npn 15 V 18 mA SOT323
V304	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V306	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V310	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223

V307	4210050	Transistor	DTA114EE	pnp RB V EM3
V308	4210052	Transistor	DTC114EE	npn RB V EM3
V591	4210052	Transistor	DTC114EE	npn RB V EM3
V602	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V604	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V607	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V712	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V520	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V501	4210074	Transistor	BFP420	npn 4. V SOT343
V791	4211288	MosFet		p–ch 12 V SOT89
V840	4219903	Transistor x 2	BFM505	npn 20 V 20V18 mA SOT363
V711	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V790	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V505	4219922	Transistor x 2		UM6
V580	4219922	Transistor x 2		UM6
V590	4219922	Transistor x 2		UM6
V603	4219922	Transistor x 2		UM6
V606	4219922	Transistor x 2		UM6
N710	4340077	IC, 1.5ghz w/b 30db/1ghz au	PC2710T	AMP
N601	4340081	IC, regulator	TK11248AM	180 mA SS06
N602	4340081	IC, regulator	TK11248AM	180 mA SS06
N603	4340081	IC, regulator	TK11248AM	180 mA SS06
N200	4340131	St5090 audio codec	tqfp44	TQFP44
N451	4340139	IC, regulator	TK11245AM	0.22 A SSO6
N820	4340147	IC, 2xsynth1.2g/510mhz ssop	LMX2332	SSOP20
D404	4340149	IC, SRAM		TSOP28
D405	4340149	IC, SRAM		TSOP28
D400	4340217	Te28f008s3 flash 3.3v 1mx8 tsop40		TSOP40
D150	4340307	IC, MCU		TQFP80
D403	4340333	IC, SRAM		TSOP32
D401	4347667	IC, EEPROM		TSOP28
N711	4350051	IC, pow.amp.		SSOP28BW
G800	4352937	Vco 1006–1031mhz 4.5v/10ma smd		SMD
N450	4370097	St7523 rfi2 v4.2 tdma codec qfp64		QFP64
D151	4370101	Cf70131 gsm/pcn asic bart sqfp144		SQFP144
D152	4370163	IC, tms320lc541 3v gj7 sqfp1 DSP		SQFP100
N300	4370225	Stt261c pscld e pw supply tqfp64		TQFP64
N551	4370243	Crfrt_st tx.mod+rxif+pwc sqfp44		SQFP44
B150	4510003	Crystal	32.768 k	+–20PPM 8x3.8
Z551	4510009	Cer.filt 13+–0.09mhz	7.2x3.2	7.2x3.2
Z505	4510065	Saw filter	947.5+–12.5 M	4X4
Z714	4510067	Saw filter	902.5+–12.5 M	4X4
G801	4510133	VCTCXO	13.00 M	+–5PPM 4.7V 2MA
Z541	4511026	Saw filter	71+–0.08 M	14.2x8.4
Z500	4512061	Dupl 890–915/935–960mhz	20x14	20x14
X102	5409033	Sim card reader ccm04–5004 2x3smd		2x3smd
X100	5469007	Syst.conn 12af+jack+dc dct2 smd		SMD

X101	5469204	SM, conn 2x15 m p0.8 pcb/pcb 2.8		2.8MM
X501	9510262	Antenna clip		3D25516 NHE–6
X500	9780172	Antenna cable w500 dmd00071		
	9854047	PCB GJ8_XX 127.5X43.0X1.0 M8 3/PA		
	9854047	PC board	GJ8_XX	127.5x43.0x1.0 m8 3/p3/PA

Parts list of GJ8A (EDMS Issue 4.1 Code: 0201017 for layout version 02)

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R103	1430001	Chip resistor	100	5 % 0.063 W 0603
R106	1430009	Chip resistor	220	5 % 0.063 W 0603
R308	1430027	Chip resistor	2.43 k	1 % 0.063 W 0603
R309	1430027	Chip resistor	2.43 k	1 % 0.063 W 0603
R216	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R217	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R219	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R220	1430029	Chip resistor	12.1 k	0.5 % 0.063 W 0603
R112	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R745	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R746	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R525	1430700	Chip resistor	10	5 % 0.063 W 0402
R558	1430700	Chip resistor	10	5 % 0.063 W 0402
R713	1430700	Chip resistor	10	5 % 0.063 W 0402
R740	1430700	Chip resistor	10	5 % 0.063 W 0402
R506	1430710	Chip resistor	22	5 % 0.063 W 0402
R514	1430710	Chip resistor	22	5 % 0.063 W 0402
R541	1430710	Chip resistor	22	5 % 0.063 W 0402
R743	1430710	Chip resistor	22	5 % 0.063 W 0402
R829	1430710	Chip resistor	22	5 % 0.063 W 0402
R831	1430710	Chip resistor	22	5 % 0.063 W 0402
R832	1430710	Chip resistor	22	5 % 0.063 W 0402
R845	1430710	Chip resistor	22	5 % 0.063 W 0402
R847	1430710	Chip resistor	22	5 % 0.063 W 0402
R595	1430710	Chip resistor	22	5 % 0.063 W 0402
R214	1430710	Chip resistor	22	5 % 0.063 W 0402
R218	1430710	Chip resistor	22	5 % 0.063 W 0402
R231	1430710	Chip resistor	22	5 % 0.063 W 0402
R232	1430710	Chip resistor	22	5 % 0.063 W 0402
R331	1430714	Chip resistor	33	5 % 0.063 W 0402
R332	1430714	Chip resistor	33	5 % 0.063 W 0402
R151	1430718	Chip resistor	47	5 % 0.063 W 0402
R152	1430718	Chip resistor	47	5 % 0.063 W 0402
R221	1430718	Chip resistor	47	5 % 0.063 W 0402
R222	1430718	Chip resistor	47	5 % 0.063 W 0402
R324	1430718	Chip resistor	47	5 % 0.063 W 0402
R327	1430718	Chip resistor	47	5 % 0.063 W 0402
R342	1430718	Chip resistor	47	5 % 0.063 W 0402
R453	1430718	Chip resistor	47	5 % 0.063 W 0402
R703	1430718	Chip resistor	47	5 % 0.063 W 0402
R744	1430718	Chip resistor	47	5 % 0.063 W 0402
R115	1430726	Chip resistor	100	5 % 0.063 W 0402
R203	1430726	Chip resistor	100	5 % 0.063 W 0402

R204	1430726	Chip resistor	100	5 % 0.063 W 0402
R305	1430726	Chip resistor	100	5 % 0.063 W 0402
R306	1430726	Chip resistor	100	5 % 0.063 W 0402
R322	1430726	Chip resistor	100	5 % 0.063 W 0402
R323	1430726	Chip resistor	100	5 % 0.063 W 0402
R510	1430726	Chip resistor	100	5 % 0.063 W 0402
R524	1430726	Chip resistor	100	5 % 0.063 W 0402
R570	1430726	Chip resistor	100	5 % 0.063 W 0402
R701	1430726	Chip resistor	100	5 % 0.063 W 0402
R702	1430726	Chip resistor	100	5 % 0.063 W 0402
R781	1430726	Chip resistor	100	5 % 0.063 W 0402
R784	1430726	Chip resistor	100	5 % 0.063 W 0402
R503	1430732	Chip resistor	180	5 % 0.063 W 0402
R801	1430732	Chip resistor	180	5 % 0.063 W 0402
R107	1430734	Chip resistor	220	5 % 0.063 W 0402
R502	1430734	Chip resistor	220	5 % 0.063 W 0402
R513	1430734	Chip resistor	220	5 % 0.063 W 0402
R564	1430734	Chip resistor	220	5 % 0.063 W 0402
R568	1430734	Chip resistor	220	5 % 0.063 W 0402
R574	1430734	Chip resistor	220	5 % 0.063 W 0402
R844	1430734	Chip resistor	220	5 % 0.063 W 0402
R596	1430734	Chip resistor	220	5 % 0.063 W 0402
R521	1430734	Chip resistor	220	5 % 0.063 W 0402
R559	1430738	Chip resistor	270	5 % 0.063 W 0402
R594	1430738	Chip resistor	270	5 % 0.063 W 0402
R598	1430738	Chip resistor	270	5 % 0.063 W 0402
R742	1430738	Chip resistor	270	5 % 0.063 W 0402
R557	1430740	Chip resistor	330	5 % 0.063 W 0402
R329	1430744	Chip resistor	470	5 % 0.063 W 0402
R343	1430744	Chip resistor	470	5 % 0.063 W 0402
R547	1430744	Chip resistor	470	5 % 0.063 W 0402
R741	1430744	Chip resistor	470	5 % 0.063 W 0402
R782	1430746	Chip resistor	560	5 % 0.063 W 0402
R101	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R109	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R202	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R205	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R261	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R262	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R263	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R264	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R270	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R300	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R301	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R304	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R312	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R314	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R326	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R330	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R560	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R562	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R563	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R792	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R834	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R840	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R565	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R780	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R783	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R785	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R200	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R207	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R260	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R265	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R266	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R267	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R268	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R269	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R452	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R522	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R571	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R586	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R609	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R714	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R717	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R795	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R830	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R843	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R523	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R790	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R794	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R797	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R587	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R584	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R720	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R820	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R821	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R105	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R501	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R511	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R605	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R608	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R718	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R791	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R823	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R824	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R825	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402

R841	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R842	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R153	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R150	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R710	1430772	Chip resistor	5.6 k	5 % 0.063 W 0402
R551	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R553	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R554	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R556	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R715	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R800	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R583	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R588	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R102	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R104	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R111	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R206	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R208	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R315	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R316	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R317	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R318	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R321	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R458	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R500	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R504	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R505	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R552	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R555	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R573	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R591	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R592	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R597	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R601	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R602	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R604	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R606	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R611	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R712	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R833	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R808	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R827	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R828	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R719	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R215	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R303	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R576	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R580	1430790	Chip resistor	27 k	5 % 0.063 W 0402

R822	1430790	Chip resistor	27 k	5 % 0.063 W 0402
R113	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R572	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R578	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R577	1430794	Chip resistor	39 k	5 % 0.063 W 0402
R311	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R313	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R589	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R716	1430800	Chip resistor	68 k	5 % 0.063 W 0402
R114	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R155	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R201	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R302	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R400	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R401	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R402	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R403	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R404	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R405	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R406	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R407	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R408	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R409	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R410	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R411	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R412	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R413	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R414	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R507	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R508	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R603	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R607	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R610	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R612	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R613	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R614	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R456	1430820	Chip resistor	470 k	5 % 0.063 W 0402
R319	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R328	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R512	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R585	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R457	1800659	NTC resistor	47 k	10 % 0.12 W 0805
R711	1800673	NTC resistor	15 k	10 % 0.12 W 0805
R116	1825001	Chip varistor vwm18v vc40v	0603	0603
R117	1825001	Chip varistor vwm18v vc40v	0603	0603
R118	1825001	Chip varistor vwm18v vc40v	0603	0603
R725	1825003	Chip varistor vwm5.5v vc15.5	0805	0805
V100	1825007	Chip varistor vwm18v vc39v	1210	1210

C304	2309570	Ceramic cap.		Y5 V 1206
C331	2309570	Ceramic cap.		Y5 V 1206
C821	2310209	Ceramic cap.	2.2 n	5 % 50 V 1206
C823	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C317	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C332	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C336	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C450	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C452	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C743	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C732	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C745	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C225	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C308	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C309	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C335	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C203	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C206	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C219	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C337	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C572	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C210	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C211	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C840	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C710	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C500	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C513	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C507	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C502	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C506	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C518	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C713	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C721	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C847	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C722	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C825	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C712	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C826	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C862	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C850	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C591	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C718	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C846	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C158	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C159	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C551	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C851	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C520	2320538	Ceramic cap.	12 p	5 % 50 V 0402

C843	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C107	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C112	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C201	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C204	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C221	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C223	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C229	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C302	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C314	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C338	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C339	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C505	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C514	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C522	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C590	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C593	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C595	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C714	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C719	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C723	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C724	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C728	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C742	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C780	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C781	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C782	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C783	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C845	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C863	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C563	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C564	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C711	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C224	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C102	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C103	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C104	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C106	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C108	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C152	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C154	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C157	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C162	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C165	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C169	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C170	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C207	2320560	Ceramic cap.	100 p	5 % 50 V 0402

C212	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C215	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C216	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C226	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C250	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C251	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C252	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C253	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C254	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C255	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C256	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C257	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C258	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C259	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C260	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C313	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C460	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C503	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C504	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C516	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C523	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C552	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C553	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C557	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C558	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C561	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C716	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C717	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C820	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C822	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C824	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C830	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C833	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C842	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C214	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C554	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C555	2320564	Ceramic cap.	150 p	5 % 50 V 0402
C545	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C546	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C574	2320568	Ceramic cap.	220 p	5 % 50 V 0402
C791	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C213	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C217	2320588	Ceramic cap.	1.5 n	5 % 50 V 0402
C573	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C844	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C801	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C101	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C151	2320620	Ceramic cap.	10 n	5 % 16 V 0402

C156	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C161	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C164	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C166	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C167	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C168	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C303	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C306	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C310	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C311	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C315	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C318	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C321	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C323	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C325	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C326	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C333	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C400	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C401	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C402	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C403	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C404	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C405	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C406	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C407	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C454	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C459	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C230	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C110	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C111	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C105	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C153	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C227	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C228	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C301	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C319	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C330	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C517	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C526	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C562	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C568	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C715	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C741	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C744	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C809	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C834	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C849	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402

C171	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C457	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C556	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C559	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C560	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C602	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C603	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C608	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C202	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C205	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C515	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C525	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C541	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C569	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C570	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C571	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C740	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C784	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C829	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C832	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C854	2320756	Ceramic cap.	3.3 n	10 % 50 V 0402
C800	2604079	Tantalum cap.	0.22 u	20 % 35 V 3.2x1.6x1.6
C729	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C601	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C604	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C605	2604329	Tantalum cap.	4.7 u	20 % 10 V 3.5x2.8x1.9
C320	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C322	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C324	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C300	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C305	2610005	Tantalum cap.	10 u	20 % 16 V 3.5x2.8x1.9
C160	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C200	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C208	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C218	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C220	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C307	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C316	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C329	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C458	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C806	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C841	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C730	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C731	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C734	2610125	Tantalum cap.	68 u	20 % 16 V 7.3x4.3x2.9
C150	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C155	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C163	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2

C456	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C828	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
C831	2610200	Tantalum cap.	2.2 u	20 % 2.0x1.3x1.2
L523	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L524	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L311	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L312	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L102	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L103	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L104	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L105	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L106	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L150	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L152	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L153	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L201	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L202	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L203	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L204	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L205	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L306	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L451	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L100	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L101	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L107	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L108	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L300	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L712	3641262	Ferrite bead 30r/100mhz 2a 1206		1206
L800	3641324	Chip coil	10 u	10 % Q=25/2.52 MHz 1008
L711	3641522	Chip coil	6 n	20 % Q=50/250 MHz 0805
L500	3643003	Chip coil	12 n	5 % Q=30/250 MHz 0805
L551	3643021	Chip coil	47 n	5 % Q=40/200 MHz 0805
L841	3643021	Chip coil	47 n	5 % Q=40/200 MHz 0805
L520	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L709	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L710	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L840	3643023	Chip coil	68 n	5 % Q=40/200 MHz 0805
L521	3643037	Chip coil	180 n	5 % Q=35/100 MHz 0805
L545	3643037	Chip coil	180 n	5 % Q=35/100 MHz 0805
L522	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L543	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
L544	3643039	Chip coil	220 n	5 % Q=35/100 MHz 0805
V780	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V842	4110062	Cap. diode	BB535	30 V 2.1/18.7PFSOD323
V511	4110083	Schdix4 bat15–099r ring	sot143	SOT143
V301	4110130	Zener diode	BZX84	2 % 5.1 V 0.3 W SOT23
V592	4112464	Pindix2 bar64–04 200v 0.1a	sot23	SOT23
V305	4115804	Schottky diode	PRLL5817	20 V 1 A SOD87

V200	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V302	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V303	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V309	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V311	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V608	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V830	4200917	Transistor	BC848B/BCW32	npn 30 V 100 mA SOT23
V512	4210011	Transistor	BFS505	npn 15 V 18 mA SOT323
V304	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V306	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V310	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V307	4210050	Transistor	DTA114EE	pnp RB V EM3
V308	4210052	Transistor	DTC114EE	npn RB V EM3
V591	4210052	Transistor	DTC114EE	npn RB V EM3
V602	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V604	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V607	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V712	4210054	Transistor	FMMT589	pnp 30 V 1 A SOT23
V520	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V150	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V501	4210074	Transistor	BFP420	npn 4. V SOT343
V791	4211288	MosFet		p–ch 12 V SOT89
V840	4219903	Transistor x 2	BFM505	npn 20 V 20V18 mA SOT363
V711	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V790	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V505	4219922	Transistor x 2		UM6
V580	4219922	Transistor x 2		UM6
V590	4219922	Transistor x 2		UM6
V603	4219922	Transistor x 2		UM6
V606	4219922	Transistor x 2		UM6
N710	4340077	IC, 1.5ghz w/b 30db/1ghz au	PC2710T	AMP
N601	4340081	IC, regulator	TK11248AM	180 mA SS06
N602	4340081	IC, regulator	TK11248AM	180 mA SS06
N603	4340081	IC, regulator	TK11248AM	180 mA SS06
N200	4340131	St5090 audio codec	tqfp44	TQFP44
N451	4340139	IC, regulator	TK11245AM	0.22 A SSO6
N820	4340147	IC, 2xsynth1.2g/510mhz ssop	LMX2332	SSOP20
D404	4340149	IC, SRAM		TSOP28
D405	4340149	IC, SRAM		TSOP28
D400	4340217	Te28f008s3 flash 3.3v 1mx8 tsop40		TSOP40
D150	4340307	IC, MCU		TQFP80
D403	4340333	IC, SRAM		TSOP32
D401	4347667	IC, EEPROM		TSOP28
N711	4350051	IC, pow.amp.		SSOP28BW
G800	4352937	Vco 1006–1031mhz 4.5v/10ma	smd	SMD
N450	4370097	St7523 rfi2 v4.2 tdma codec qfp64		QFP64
D151	4370101	Cf70131 gsm/pcn asic bart sqfp144		SQFP144

D152	4370163	IC, tms320lc541 3v gj7 sqfp1 DSP	SQFP100
N300	4370223	Stt261c pscld_e pw supply tqfp44	TQFP44
N551	4370243	Crfrt_st tx.mod+rxif+pwc sqfp44	SQFP44
B150	4510003	Crystal 32.768 k	+–20PPM 8x3.8
Z551	4510009	Cer.filt 13+–0.09mhz 7.2x3.2	7.2x3.2
Z505	4510065	Saw filter 947.5+–12.5 M	4X4
Z714	4510067	Saw filter 902.5+–12.5 M	4X4
G801	4510133	VCTCXO 13.00 M	+–5PPM 4.7V 2MA
Z541	4511026	Saw filter 71+–0.08 M	14.2x8.4
Z500	4512061	Dupl 890–915/935–960mhz 20x14	20x14
X102	5409033	Sim card reader ccm04–5004 2x3smd	2x3smd
X100	5469007	Syst.conn 12af+jack+dc dct2 smd	SMD
X101	5469204	SM, conn 2x15 m p0.8 pcb/pcb 2.8	2.8MM
X501	9510262	Antenna clip	3D25516 NHE–6
X500	9780172	Antenna cable w500 dmd00071	
	9854187	PCB GJ8A 127.5X43.0X1.0 M8 3/PA	
	9854187	PC board GJ8A	127.5x43.0x1.0 m8 3/pa

This page intentionally left blank.